Plasmonic Logic Gates at Optimum Optical Communications Wavelength

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ABSTRACT This paper displays a design that realizes all optical logic gates (NOT, AND, OR, NAND, NOR, XOR, XNOR) and consisting of one nanoring and four strips Operates on the principle of resonance. the proposed design works at the wavelength of 1550 nm using insulator-metal-insulator (IMI) plasmonic waveguide. The basic principle of the operation of these gates is input and control signals' constructive and destructive interference. The proposed transmission threshold's value is 0.25 between OFF state and ON state. The proposed design has small dimensions (300 nm × 300 nm) and can realize seven logic gates with maximum transmission 134% at NOT gate, 223% at OR gate, 134% at NAND gate and 223% at XNOR gate where the design is optimum and the modulation depth is very high because it's ranges in all gates more than 90%. The proposed structure contributes in building nanocircuits for integrated photonic circuits and optical signal processing.

INDEX TERMS Nanophotonics, Plasmonics, Logic Devices.

I. INTRODUCTION

In previous years, clear advances have emerged in the field of All-optical devices due to research efforts and studies of surface plasmon polaritons (SPPs) field [1]. SPP All-optical devices, which represent applications of plasmonic phenomena, were able to overcome the problems found in optical devices such as the diffraction limit that appears when the device's size is close to or greater than the light's wavelength that limits the minimum chip size [2], as well as the problems of electronic devices such as low data rate, low speed and heat generation that rises as a result of increased resistance [3], [4], which leads to inability to apply the principle of high frequency and transfer data at a high rate. SPPs represents the interaction between free electrons of metals and electromagnetic waves and propagation happens on metal-dielectric interface as the electrons oscillate at the light frequencies [5], [6], [7]. Various plasmonic devices such as resonators [8], splitters [9], modulators [10], switches [11], [12], and logic gates [13], [14] were manufactured. Lots of studies have been created on logic gates, so different designs have been created made of different materials and with different geometric shapes and resonance frequencies, each design achieves a certain number of logic gates such as one design it's dimensions (2.4 μm × 3 μm) provides one logic gate when the wavelength is 850 nm [15], one design it's dimensions (760 nm × 600 nm) provides three logic gates when the wavelength is 1535 nm [16], two design their dimensions (1220 nm × 1120 nm) provide four logic gates when the wavelength is 525 nm [17], two design their dimensions (750 nm × 900 nm and 1.5 μm × 1.8 μm) provide three logic gates when the wavelength is 1535 nm [18], one design it's dimensions (400 nm × 400 nm) provides seven logic gates when the wavelength is 1550 nm [3], and one design it's dimensions (400 nm × 380 nm) provides seven logic gates when the wavelengths is 900 nm and 1330 nm [19].

In this paper, we suggest a new design with small dimensions (300 nm × 300 nm) that could achieve the seven logic gates (NOT, AND, OR, NAND, NOR, XOR, XNOR) where maximum transmission 134% at NOT gate, 223% at OR gate, 134% at NAND gate, and 223% at XNOR gate where the design is optimum design based on modulation depth equation and its resonance frequency at the wavelength of 1550 nm and with a transmission threshold 0.25 for all gates. The design efficiency and performance of the gates were measured by three standards: transmission, contrast ratio, and modulation depth.

We organized this paper as following: Section 2 explains the structure design, theoretical concept and material. Section 3 explains the performance and simulation results for plasmonic logic gates. Section 4 explains the difference between the proposed work and previous research. Section 5 explains the concluding remarks.

II. THEORETICAL CONCEPT AND STRUCTURE LAYOUT

The proposed design that was designed to realize the seven plasmonic logic gates is illustrated at Fig. 1. This design consists of one nanoring resonator in the middle and four straight strips around it. The nanoring resonator and strips formed from silver as a conductor, while the rest of the design made of low refractive index dielectric material (crystal). Since all the seven gates have same parameters, materials and dimensions in their structure, Table I provides the proposed design's dimensions.
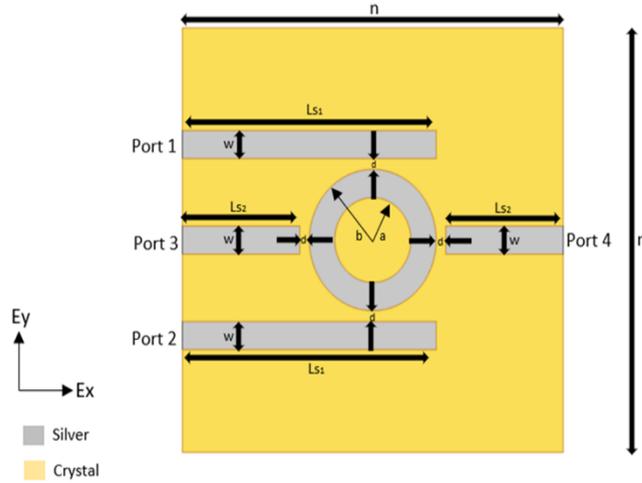

FIGURE 1. Proposed design that achieves the proposed seven plasmonic logic gates.

TABLE I. Proposed model's parameters

Parameter	Value
n	300 nm
L_{S_1}	200 nm
L_{S_2}	92.5 nm
w	20 nm
a	30 nm
b	50 nm
d	7.5 nm

All optical logic gates realized in one design by relying on insulator - metal - insulator (IMI) plasmonic waveguides in lieu of metal - insulator - metal (MIM) plasmonic waveguides because of its advantages such as less propagation loss, less confinement, high propagation length, high quality factor, low coupling loss and easy fabrication [3]. The refractive index of low refractive index dielectric material (crystal) is equal to 1.926 [20], while the silver used in the composition of the nanoring resonator and the four strips was according to Johnson and Christie's data. The value of the nanoring resonance wavelength λ_{sp} is calculated by the equation below [3].

$$\lambda_{sp} = 4\pi n_{eff} D \qquad (1)$$

Where the effective refractive index is symbolized by n_{eff} and the larger diameter of the nanoring is symbolized by D. Given that the wavelength of 1550 nm is the best option in optical communication applications, it was adopted in this research where the proposed design was designed with specific dimensions and types of materials that fit the chosen wavelength of resonance. For the transverse magnetic mode (TM), the dispersion equation is given as [3], [21].

$$\varepsilon_m k_d + \varepsilon_d k_m \tan h \left(w \frac{k_m}{2}\right) = 0 \qquad (2)$$

Metal dielectric constant is symbolized by ε_m, dielectric wave number is symbolized by k_d, the insulator dielectric constant is symbolized by ε_d, metal wave number is symbolized by k_m, and the thickness of the metal is symbolized by W.

$$k_d = (\beta^2 + \varepsilon_d k_0^2)^{\frac{1}{2}} \qquad (3)$$

$$k_m = (\beta^2 + \varepsilon_m k_0^2)^{\frac{1}{2}} \qquad (4)$$

$$k_0 = \frac{2\pi}{\lambda} \qquad (5)$$

Free space wave number is symbolized by k_0 and the propagation constant is symbolized by β which is represented by n_{eff} of the waveguide such as [3], [16].

$$n_{eff} = \frac{\beta}{k_0} \qquad (6)$$

Two-dimensional (2-D) Finite element method (FEM) is method in which performance of the system is measured and Maxwell's equations are solved numerically. convolutional perfectly matched layer used as the absorbing boundary condition simulate the computational area. The proposed design has four ports, two of which are for the input, one for the control and one for the output, which are specified by the type of gate. A polarized waveform (TM) with an electromagnetic field for the E_X, E_Y and H_Z components Is exposed to input ports. The proposed design achieves all seven logic gates with the same dimensions and materials for all gates. A transmission threshold of 0.25 was chosen between ON state and OFF state [22]. Performance of logic gates and proposed design is measured by three standard: The first standard is the transmission T, which is measured for the two states of ON and OFF [3]. The transmission threshold is a criterion for determining the type of the state where the transmission value must be greater than 0.25 for all gates in ON state [22]. the transmission value is measured by the equation [15], [16].

$$T = \frac{P_{out}}{P_{in}} \qquad (7)$$

Where the transmission is symbolized by T, the output optical power is symbolized by P_{out}, and optical power of input that entered into control port or single input port, which is 1 µW, is symbolized by P_{in}.

The second standard is optical power's contrast ratio (CR) in ON-OFF state at the output port that is described as shown in Table II [23], so when the difference in power is large, the performance of the gate is high. the following equation explains the mechanism for calculating the contrast ratio [16], [19].

$$cr\ (dB) = 10lo\ g\left(\frac{P_{out-ON(min)}}{P_{out-OFF(max)}}\right) \qquad (8)$$

The output optical power's minimal value in ON state is symbolized by $P_{out-ON(min)}$, while the output optical power's maximum value in OFF state is symbolized by $P_{out-OFF(max)}$.

TABLE II. Describe values of contrast ratio

Contrast ratio (dB) ranges	Description	Performance
Negative value	Low	Poor and inefficient
Less than or equal 4 dB	Low	Accepted
More than 4 to 8 dB	Medium	Moderate
More than 8 to 12 dB	Medium	Good and efficient
More than 12 to 16 dB	High	Very good and efficient
More than 16 to 20 dB	High	Excellent and efficient
More than 20 dB	Very high	Excellent and very efficient

The third standard is the modulation depth (MD) that is described as shown in table III, where the efficiency of the design dimensions is measured according to the following equation [24], [25].

$$MD = \left(\frac{T_{ON\ (max)} - T_{OFF(min)}}{T_{ON(max)}}\right) \times 100\% \qquad (9)$$

The maximum value of the transmission in ON state is symbolized by $T_{ON(max)}$ and the transmission's minimum value in OFF state is symbolized by $T_{OFF(min)}$.

TABLE III. Describe the modulation depth values

Modulation Depth Ranges	DESCRIPTION	Optimality in Dimensions
Less than 10 %	Low	Poor and Inefficient
10 %-Less than 20 %	Low	Accepted
20 % - Less than 40 %	Medium	Moderate
40 % - Less than 60 %	Medium	Good and Efficient
60 % - Less than 80 %	High	Very good and Efficient
80 % - Less than 90 %	High	Excellent and Efficient
More than 90 %	Very High	Excellent and Optimum

Surface resonance occurs because of the interaction between the metallic plasmonic nanoring and the strips due to the coupling of the electromagnetic fields between the nanoring resonator and the strips. Transmission power depends on the dimensions of the parameters of the design and their distance from each other and the type of materials the design is made of, as one design with the same dimensions and materials achieves all gates, but the difference between one gate and another lies in manipulating and changing the ports, as well as changing the angles of input power in control and input ports to form constructive and destructive interference which submit to the incident wave phase as in the equation below [26].

$$m = \frac{4\ n_{eff}\ d\ cos\theta}{\lambda} \qquad (10)$$

m represents a number greater than 0 describing the phase of the interference, the effective refractive index is symbolized by n_{eff}, thickness of the metal is symbolized by d, phase is symbolized by θ, and incident wavelength is symbolized by λ. It is worth noting that changing the phase angle of the signals that inputted to the control port and the input port need a pre-controller circuit before entering the structure, and this is not discussed in this paper.

III. PROPOSED ALL OPTICAL LOGIC GATES

Trial-and-error is the method used in choosing input, control and output ports for all logic gates in order to get the best transmission, contrast ratio and modulation depth. The transmission light that the input and control ports are exposed to in all optical gates has a wavelength range from 800 nm to 2000 nm.

A. PLASMONIC NOT GATE

NOT logic gate acts like a reflector for its input signal as shown in the truth table at the Fig. 2 (a). Fig. 2 (b) shows the circuit symbol. To achieve NOT gate port 3 was considered as input port, port 1 as first control port, port 2 as second control port and port 4 as output port in NOT gate design as shown in Fig. 1. Arranging the ports in this way leads to destructive and constructive interference between the control and input signals. The state of output port is ON which is higher than the transmission threshold when input port's state is OFF and control ports are in ON state and in the same phase. When input port's state is ON and the control ports are also ON state and operate with a phase difference for all ports, the output port's state will be OFF which is less than the value of the transmission threshold. Proposed plasmonic NOT gate's transmission spectra are shown at Fig. 2 (c). Magnetic field distribution of the first and the second cases are shown at Fig. 3 (a) and Fig. 3 (b), respectively. Table IV shows the value of

transmission and input phase, table V shows contrast ratio's value, and table VI shows the value of the modulation depth. The contrast ratio is high because of $(P_{out-ON(min)})$ is higher than $(P_{out-OFF(max)})$ and the contrast is large between the values of these optical powers. Thus, the performance of this proposed gate is excellent and efficient. The modulation depth is very high because the variance between the maximum transmission in ON state and the minimum transmission in OFF state is very large. As a result, the dimensions of the proposed design are excellent and optimum.
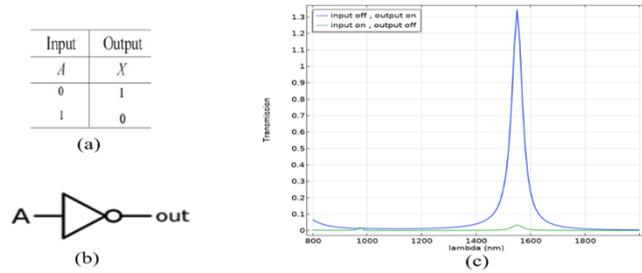

FIGURE 2. (a) NOT gate truth table, (b) NOT gate conventional symbol, and (c) Transmission spectra of proposed plasmonic NOT gate for ON and OFF states.
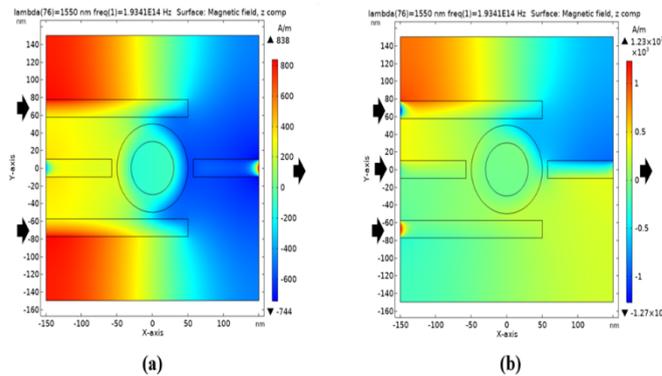

FIGURE 3. Proposed plasmonic NOT gate magnetic field distribution: (a) first case and (b) second case.

TABLE IV. Operation of proposed plasmonic NOT gate's transmission

i/p port	PHASE (DEG)	Control port 1	Phase (deg)
OFF	0	ON	0
ON	90	ON	180

TABLE IV. Operation of proposed plasmonic NOT gate's transmission continued

Control port 2	PHASE (DEG)	T	Tth	o/p port
ON	0	1.34	0.25	ON
ON	0	0.03	0.25	OFF

TABLE V. Contrast ratio for proposed plasmonic NOT gate

Pout(on-min)(µW)	Pout(off-max)(µW)	Contrast ratio (dB)
1.34	0.03	16.49

TABLE VI. Modulation depth for proposed plasmonic NOT gate

T(on-max) (µW)	T(off-min) (µW)	Modulation depth
1.34	0.03	97.76%

B. PLASMONIC AND GATE

AND logic gate has four logical states, three of which are OFF and one is ON. If all the inputs are ON, the output is ON, otherwise the output is OFF as shown in the truth table in Fig. 4 (a). Fig. 4 (b) shows the circuit symbol. To achieve AND gate port 1 was considered as the first input port, port 2 as the second input port, port 4 as control port and port 3 as output port in the proposed design as shown in Fig. 1. Constructive interference only occurs when all the inputs are ON and in the same phase where the transmission value is higher than the transmission threshold value. If the two inputs are opposite, the interference is destructive. The control port is always ON and at angle of 0°. Proposed plasmonic AND gate's transmission spectra are shown in Fig. 4 (c). Magnetic field distribution of all cases is illustrated in Fig. 5 (a), Fig. 5 (b), Fig. 5 (c), and Fig. 5 (d), respectively. Table VII Shows the value of transmission, table VIII shows the value of the Contrast Ratio, and table IX shows the value of modulation depth. The contrast ratio is medium because the contrast between $(P_{out-ON(min)})$ and $(P_{out-OFF(max)})$ is not large enough. Thus, the performance of this proposed gate is good and efficient. The modulation depth is very high because the variance between the maximum transmission in ON state and the minimum transmission in OFF state is very large. As a result, the dimensions of the proposed design are excellent and optimum.
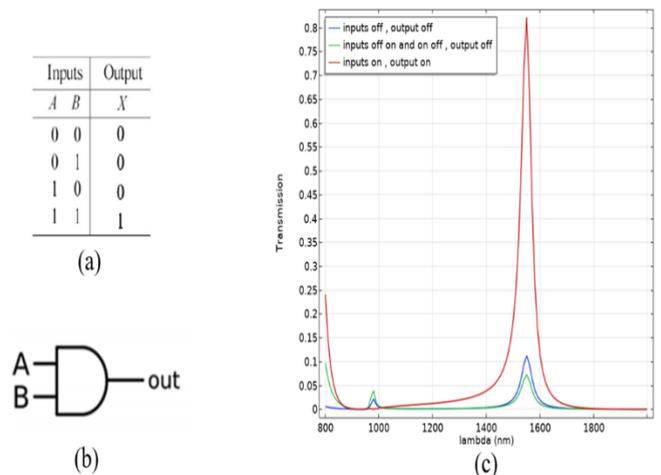

FIGURE 4. (a) AND gate truth table, (b) AND gate conventional symbol, and (c) Transmission spectra of proposed plasmonic AND gate at the four states.
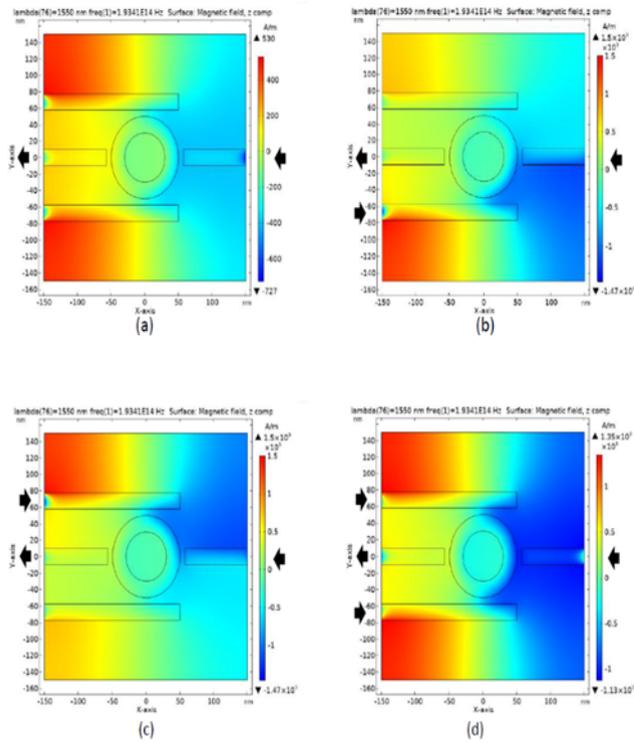
FIGURE 5. Proposed plasmonic AND gate magnetic field distribution: (a) the first case, (b) the second case, (c) the third case, and (d) the fourth case.

TABLE VII. Operation of proposed plasmonic AND gate's transmission

i/p port 1	PHASE (DEG)	i/p port 2	Phase (deg)
OFF	0	OFF	0
OFF	0	ON	180
ON	180	OFF	0
ON	0	ON	0

TABLE VII. Operation of proposed plasmonic AND gate's transmission continued

Control port	PHASE (DEG)	T	Tth	o/p port
ON	0	0.11	0.25	OFF
ON	0	0.07	0.25	OFF
ON	0	0.07	0.25	OFF
ON	0	0.82	0.25	ON

TABLE VIII. Contrast ratio for proposed plasmonic AND gate

Pout(on-min) (µW)	Pout(off-max) (µW)	Contrast ratio(dB)
0.82	0.11	8.72

TABLE IX. Modulation depth for proposed plasmonic AND gate

| T(on-max) (µW)	T(off-min) (µW)	Modulation depth
0.82	0.07	91.46%

C. PLASMONIC OR GATE

OR logic gate has four logical states, three of which are ON and one is OFF. If all the inputs are OFF, the output is OFF, otherwise the output is ON as shown in the truth table in Fig. 6 (a). Fig. 6 (b) shows the circuit symbol. To achieve OR gate port 1 was considered as the first input port, port 2 as the second input port, port 3 as the control port and port 4 as the output port in the proposed design as shown in Fig. 1. Constructive interference occurs If one or all of the inputs are ON state where the input and control port signal in same phase. the control port is always ON and at angle of 0°. Proposed plasmonic OR gate's transmission spectra are illustrated in Fig. 6 (c). Magnetic field distribution of all cases is illustrated in Fig. 7 (a), Fig. 7 (b), Fig. 7 (c), and Fig. 7 (d), respectively. Table X shows the value of transmission, table XI shows the value of the Contrast Ratio, and table XII shows the value the modulation depth. The contrast ratio is medium because the contrast between $(P_{out-ON(min)})$ and $(P_{out-OFF(max)})$ is not large enough. Thus, the performance of this proposed gate is good and efficient. The modulation depth is very high because the variance between the maximum transmission in ON state and the minimum transmission in OFF state is very large. As a result, the dimensions of the proposed design are excellent and optimum.
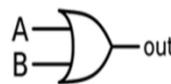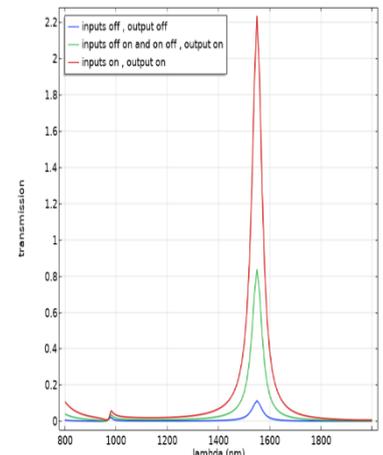
FIGURE 6. (a) OR gate truth table, (b) OR gate conventional symbol, and (c) Transmission spectra of proposed plasmonic OR gate at the four states.
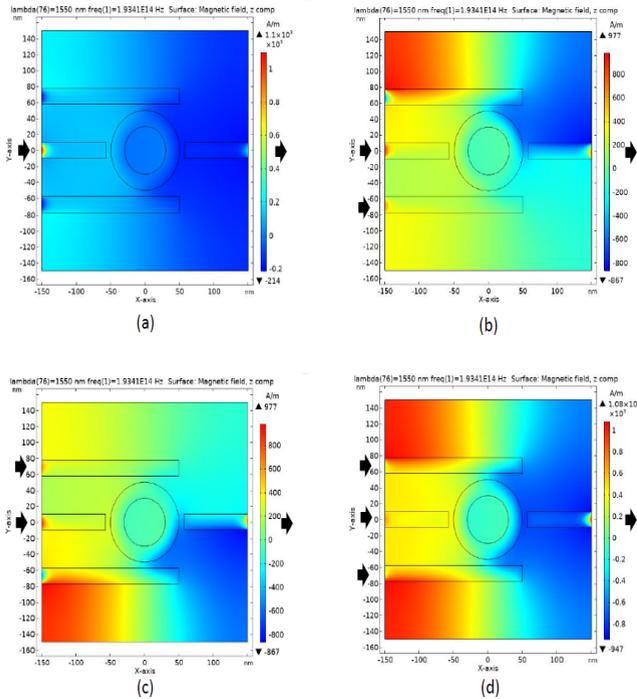
FIGURE 7. Proposed plasmonic OR gate magnetic field distribution: (a) the first case, (b) the second case, (c) the third case, and (d) the fourth case.

TABLE X. Operation of proposed plasmonic OR gate's transmission

i/p port 1	PHASE (DEG)	i/p port 2	Phase (deg)
OFF	0	OFF	0
OFF	0	ON	0
ON	0	OFF	0
ON	0	ON	0

TABLE X. Operation of proposed plasmonic OR gate's transmission continued

Control port	PHASE (DEG)	T	Tth	o/p port
ON	0	0.11	0.25	OFF
ON	0	0.83	0.25	ON
ON	0	0.83	0.25	ON
ON	0	2.23	0.25	ON

TABLE XI. Contrast ratio for proposed plasmonic OR gate

Pout(on-min)(µW)	Pout(off-max)(µW)	Contrast ratio(dB)
0.83	0.11	8.77

TABLE XII. Modulation depth for proposed plasmonic OR gate

| T(on-max) (µW)	T(off-min) (µW)	Modulation depth
2.23	0.11	95.06%

D. PLASMONIC NAND GATE

NAND logic gate has four logical states, three of which are ON and one is OFF. If all the inputs are ON, the output is OFF, the other three cases are all ON. This gate is opposite to the logic gate AND as shown in the truth table in Fig. 8 (a). Fig. 8 (b) shows the circuit symbol. To achieve NAND gate port 2 was considered as the first input port, port 3 as the second input port, port 1 as the control port and port 4 as output port in the proposed design as shown in Fig. 1. Both constructive and destructive interference play a role in achieving the function of this gate because of the phase difference between the transmitted signals. The control port is always ON and at angle of 0°. Proposed plasmonic NAND gate's transmission spectra are shown in Fig. 8 (c). Magnetic field distribution of all cases is illustrated in Fig. 9 (a), Fig. 9 (b), Fig. 9 (c), and Fig. 9 (d), respectively. Table XIII shows the value of transmission, table XIV shows the value of the Contrast Ratio, and table XV shows the value of the modulation depth. The contrast ratio is medium because the contrast between ($P_{out-ON(min)}$) and ($P_{out-OFF(max)}$) is not large enough. Thus, the performance of this proposed gate is good and efficient. The modulation depth is very high because the variance between the maximum transmission in ON state and the minimum transmission in OFF state is very large. As a result, the dimensions of the proposed design are excellent and optimum.
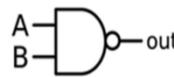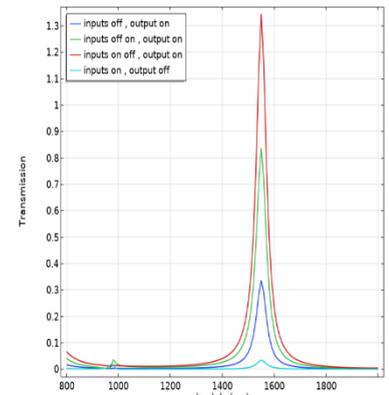
FIGURE 8. (a) NAND gate truth table, (b) NAND gate conventional symbol, and (c) Transmission spectra of proposed plasmonic NAND gate at the four states.
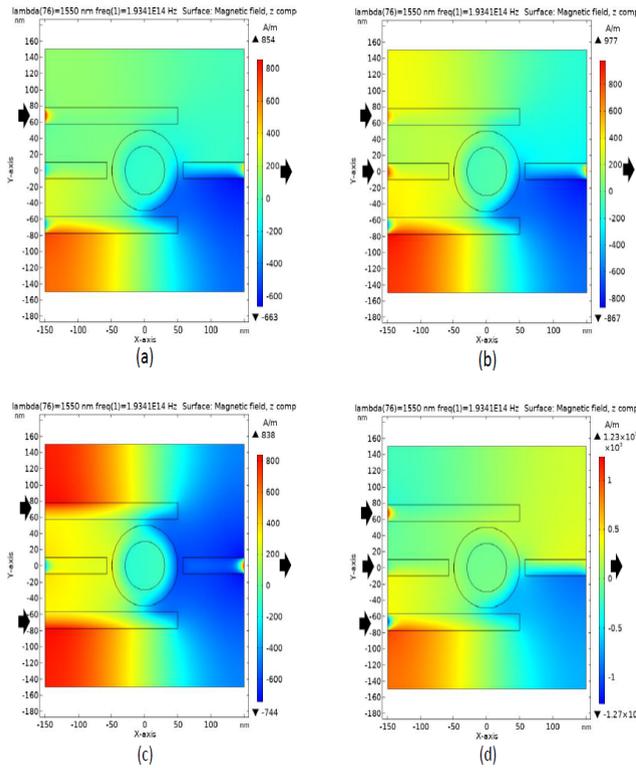
FIGURE 9. Proposed plasmonic NAND gate magnetic field distribution: (a) the first case, (b) the second case, (c) the third case, and (d) the fourth case.

TABLE XIII. Operation of proposed plasmonic NAND gate's transmission

i/p port 1	PHASE (DEG)	i/p port 2	Phase (deg)
OFF	0	OFF	0
OFF	0	ON	0
ON	0	OFF	0
ON	180	ON	90

TABLE XIII. Operation of proposed plasmonic NAND gate's transmission continued

Control port	PHASE (DEG)	T	Tth	o/p port
ON	0	0.33	0.25	ON
ON	0	0.83	0.25	ON
ON	0	1.34	0.25	ON
ON	0	0.03	0.25	OFF

TABLE XIV. Contrast ratio for proposed plasmonic NAND gate

Pout(on-min)(µW)	Pout(off-max)(µW)	Contrast ratio(dB)
0.33	0.03	10.41

TABLE XV. Modulation depth for proposed plasmonic NAND gate

| T(on-max) (µW)	T(off-min) (µW)	Modulation depth
1.34	0.03	97.76%

E. PLASMONIC NOR GATE

NOR logic gate has four logical states, three of which are OFF and one is ON. If all the inputs are OFF, the output is ON, otherwise the output is OFF. This gate is the opposite of OR logic gate as shown in the truth table in Fig. 10 (a). Fig. 10 (b) shows the circuit symbol. To achieve NOR gate port 2 was considered as the first input port, port 3 as the second input port, port 1 as the control port and port 4 as the output port in the proposed design as shown in Fig. 1. The first case of the NOR gate is very similar in its operation to the first case of NOT gate, while the rest of the cases can be achieved by destructive interference resulting from the difference in phase. The control port is always ON and at angle of (180°). Proposed plasmonic NOR gate's transmission spectra are illustrated in Fig. 10 (c). Magnetic field distribution of all cases is illustrated in Fig. 11 (a), Fig. 11 (b), Fig. 11 (c), and Fig. 11 (d), respectively. Table XVI shows the value of transmission, table XVII shows the value of the Contrast Ratio, and table XVIII Shows the value of the modulation depth. The contrast ratio is medium because the contrast between ($P_{out-ON(min)}$) and ($P_{out-OFF(max)}$) is not large enough. Thus, the performance of this proposed gate is moderate. The modulation depth is very high because the variance between the maximum transmission in ON state and the minimum transmission in OFF state is very large. As a result, the dimensions of the proposed design are excellent and optimum.
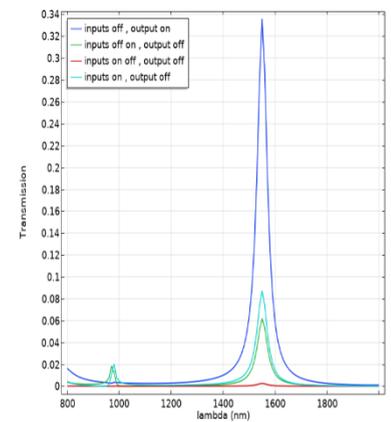
FIGURE 10. (a) NOR gate truth table, (b) NOR gate conventional symbol, and (c) Transmission spectra of proposed plasmonic NOR gate at the four states.
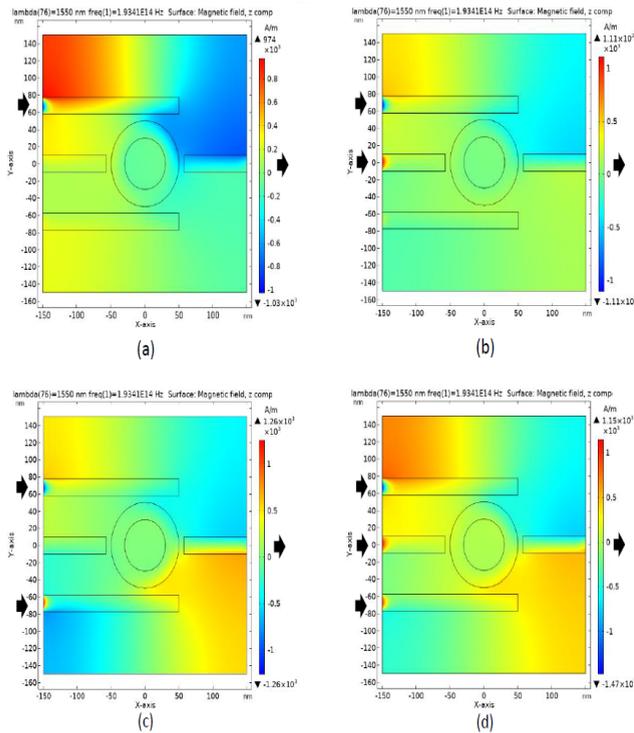
FIGURE 11. Proposed plasmonic NOR gate magnetic field distribution: (a) the first case, (b) the second case, (c) the third case, and (d) the fourth case.

TABLE XVI. Operation of proposed plasmonic NOR gate's transmission

i/p port 1	PHASE (DEG)	i/p port 2	Phase (deg)
OFF	0	OFF	0
OFF	0	ON	45
ON	45	OFF	0
ON	45	ON	0

TABLE XVI. Operation of proposed plasmonic NOR gate's transmission continued

Control port	PHASE (DEG)	T	Tth	o/p port
ON	180	0.33	0.25	ON
ON	180	0.06	0.25	OFF
ON	180	0.002	0.25	OFF
ON	180	0.08	0.25	OFF

TABLE XVII. Contrast ratio for proposed plasmonic NOR gate

Pout(on-min)(μW)	Pout(off-max)(μW)	Contrast ratio(dB)
0.33	0.08	6.15

TABLE XVIII. Modulation depth for proposed plasmonic NOR gate

T(on-max) (μW)	T(off-min) (μW)	Modulation depth
0.33	0.002	99.39%

F. PLASMONIC XOR GATE

XOR logic gate has four logical states, two of which are ON and two are OFF. If the two inputs are opposite with value (0 1, 1 0) then the output is ON, but if the two inputs are the same (00, 11) then the output is OFF as shown in the truth table in Fig. 12 (a). Fig. 12 (b) shows the circuit symbol. To achieve XOR gate port 1 was considered as the first input port, port 2 as the second input port, port 3 as the control port and port 4 as the output port in the proposed design as shown in Fig. 1. Destructive interference occurs in the fourth case only, resulting in OFF state. In second and third cases constructive interference occurs, resulting in ON state. The control port is always ON and at angle of (0°). Proposed plasmonic XOR gate's transmission spectra are illustrated in Fig. 12 (c). Magnetic field distribution of all cases is illustrated in Fig. 13 (a), Fig. 13 (b), Fig. 13 (c), and Fig. 13 (d), respectively. Table XIX shows the value of transmission, table XX shows the value of the Contrast Ratio, and table XXI Shows the value the modulation depth. The contrast ratio is medium because the contrast between $(P_{out-ON(min)})$ and $(P_{out-OFF(max)})$ is not large enough. Thus, the performance of this proposed gate is good and efficient. The modulation depth is very high because the variance between the maximum transmission in ON state and the minimum transmission in OFF state is very large. As a result, the dimensions of the proposed design are excellent and optimum.
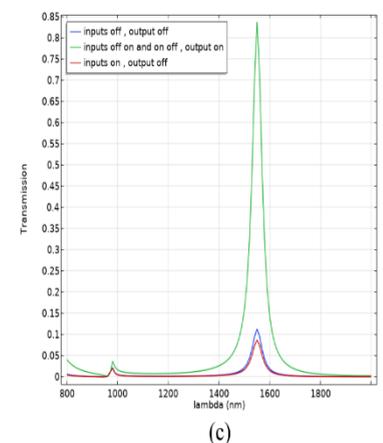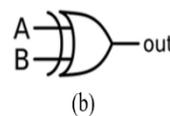

FIGURE 12. (a) XOR gate truth table, (b) XOR gate conventional symbol, and (c) Transmission spectra of proposed plasmonic XOR gate at the four states.
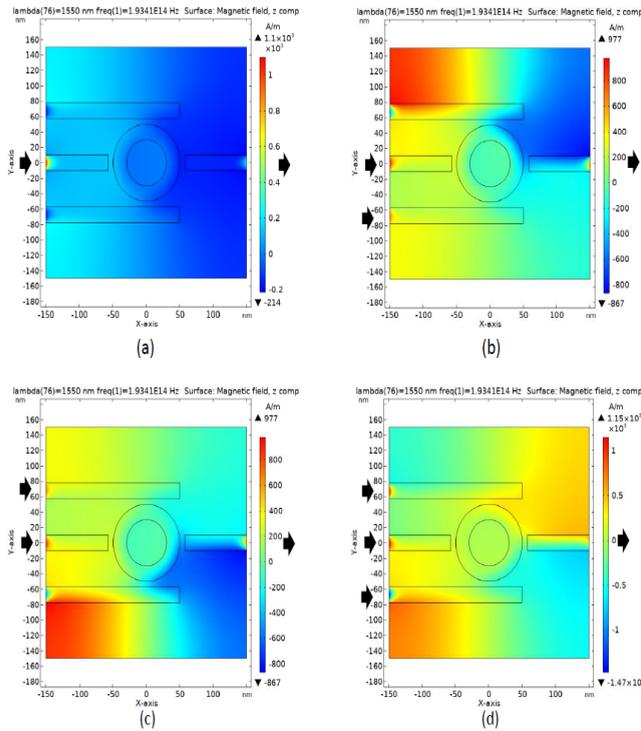
FIGURE 13. Proposed plasmonic XOR gate magnetic field distribution: (a) the first case, (b) the second case, (c) the third case, and (d) the fourth case.

TABLE XIX. Operation of proposed plasmonic XOR gate's transmission

i/p port 1	PHASE (DEG)	i/p port 2	Phase (deg)
OFF	0	OFF	0
OFF	0	ON	0
ON	0	OFF	0
ON	45	ON	180

TABLE XIX. Operation of proposed plasmonic XOR gate's transmission continued

Control port	PHASE (DEG)	T	Tth	o/p port
ON	0	0.11	0.25	OFF
ON	0	0.83	0.25	ON
ON	0	0.83	0.25	ON
ON	0	0.08	0.25	OFF

TABLE XX. Contrast ratio for proposed plasmonic XOR gate

Pout(on-min)(µW)	Pout(off-max)(µW)	Contrast ratio(dB)
0.83	0.11	8.77

TABLE XXI. Modulation depth for proposed plasmonic XOR gate

T(on-max) (µW)	T(off-min) (µW)	Modulation depth
0.83	0.08	90.36%

G. PLASMONIC XNOR GATE

XNOR logic gate has four logical states, two of which are ON and two are OFF. If the two inputs are the same with the value (00, 11) then the output is ON, but if the two inputs are opposite with the value (01, 10) then the output is OFF as shown in the truth table in Fig. 14 (a). Fig. 14 (b) shows the circuit symbol. To achieve XNOR gate Port 2 was considered as the first input port, port 3 as the second input port, port 1 as the control port and port 4 as the output port in the proposed design as shown in Fig. 1. XNOR gate ports are the same as the ports of NOR and NAND gates, but the difference lies in the angle of the input signals to achieve the desired gate. The first case of this gate is similar to the first case of the NOT gate. In the second and third cases, destructive interference occurs between control and input signals because of the phase difference leading to a transmission value less than the transmission threshold value. In fourth case, constructive interference between input and control signals leads to a transmission value greater than the transmission threshold value. The control port is always ON and at angle of (180°). Proposed plasmonic XNOR gate's transmission spectra are illustrated in Fig. 14 (c). Magnetic field distribution of all cases is illustrated in Fig. 15 (a), Fig. 15 (b), Fig. 15 (c), and Fig. 15 (d), respectively. Table XXII shows the value of transmission, table XXIII shows the value of the Contrast Ratio, and table XXIV shows the value the modulation depth. The contrast ratio is medium because the contrast between $(P_{out-ON(min)})$ and $(P_{out-OFF(max)})$ is not large enough. Thus, the performance of this proposed gate is moderate. The modulation depth is very high because the variance between the maximum transmission in ON state and the minimum transmission in OFF state is very large. As a result, the dimensions of the proposed design are excellent and optimum.
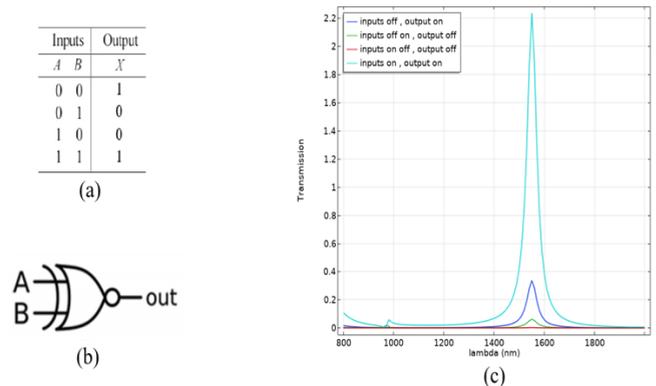

FIGURE 14. (a) XNOR gate truth table, (b) XNOR gate conventional symbol, and (c) Transmission spectra of proposed plasmonic XNOR gate at the four states.
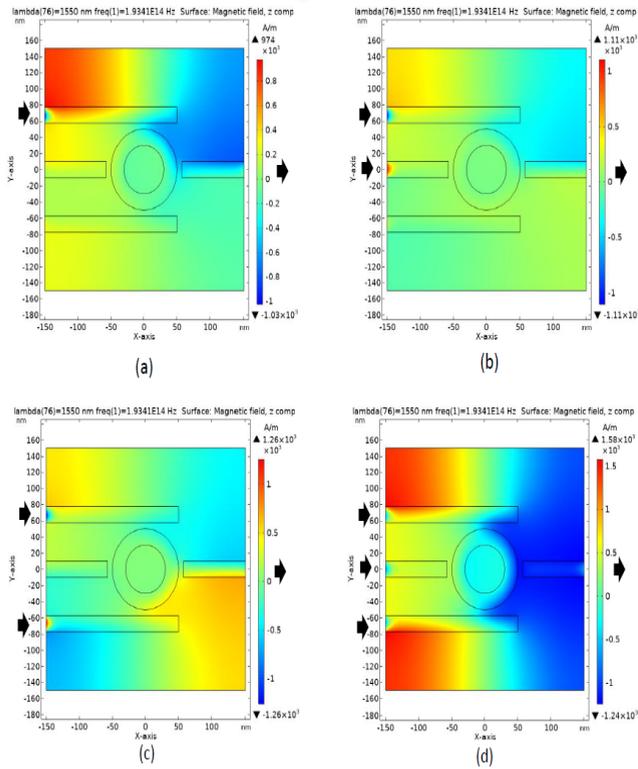
FIGURE 15. Proposed plasmonic XNOR gate magnetic field distribution: (a) the first case, (b) the second case, (c) the third case, and (d) the fourth case.

TABLE XXII. Operation of proposed plasmonic XNOR gate's transmission

i/p port 1	PHASE (DEG)	i/p port 2	Phase (deg)
OFF	0	OFF	0
OFF	0	ON	45
ON	45	OFF	0
ON	180	ON	180

TABLE XXII. Operation of proposed plasmonic XNOR gate's transmission continued

Control port	PHASE (DEG)	T	Tth	o/p port
ON	180	0.33	0.25	ON
ON	180	0.06	0.25	OFF
ON	180	0.002	0.25	OFF
ON	180	2.23	0.25	ON

TABLE XXIII. Contrast ratio for proposed plasmonic XNOR gate

Pout(on-min)(µW)	Pout(off-max)(µW)	Contrast ratio(dB)
0.33	0.06	7.4

TABLE XXIV. Modulation depth for proposed plasmonic XNOR gate

T(on-max) (µW)	T(off-min) (µW)	Modulation depth
2.23	0.002	99.91%

IV. COMPARISON BETWEEN THE PROPOSED WORK AND PREVIOUS WORKS

The comparison criteria between this work and previous works are summarized in the table XXV, which shows that the design proposed in this work has better performance than other designs in previous works according to its size, number of plasmonic logic gates, operating wavelength, and augmented transport in some states of some logic gates.

TABLE XXV. Comparison between our paper and previous papers

Criteria	REF. [15]	Ref. [16]	Ref. [17]
Proposed logic gates	NOT	NOT, OR, XOR	NOT, NAND, XOR, XNOR
Plasmonic waveguide	MIM	MIM	MIM
Number of models that realize the logic gates	One structure	One structure	Two structures
Size(s)	$2.4\mu m$ $\times 3\mu m$	$760\ nm$ $\times\ 600\ nm$	$1220\ nm$ $\times 1120\ nm$
Operating wavelength	850 nm	1535 nm	525 nm
Insulation material	Air	Air	Air
Conductive material	Ag	Ag	Ag
Maximum transmission %	NOT:65.35%	NOT:38 % OR:80 % XOR:40 %	NAND:25 % XOR:42% XNOR:25 %
Transmission's Amplifying	None	None	None
The program used in the simulation	FDTD-2-D	FDTD-2-D	FDTD-2-D
Performance measured	Transmission and contrast ratio	Transmission	Transmission
Threshold of transmission	10%	30%	35%

TABLE XXV. Comparison between our paper and previous papers continued

Criteria	REF. [3]	Ref. [19]	This paper
Proposed logic gates	All 7 logic gates	All 7 logic gates	All 7 logic gates
Plasmonic waveguide	IMI	IMI	IMI
Number of models that realize the logic gates	One structure	One structure	One structure
Size(s)	$400\,nm \times 400\,nm$	$400\,nm \times 380\,nm$	$300\,nm \times 300\,nm$
Operating wavelength	1550 nm	900 nm and 1330 nm	1550 nm
Insulation material	Teflon	Teflon	low refractive index dielectric material (crystal)
Conductive material	Ag	Ag	Ag
Maximum transmission %	NOT:28.07% OR:175% AND:72% NOR:28.07% NAND:112.3% XOR:63% XNOR:175%	At 900 nm: NOT:28% OR:239% AND:239% NOR:28.6% NAND:114% XOR:102% XNOR:239% At 1330 nm: NOT:31% OR:187% AND:182% NOR:31% NAND:124% XOR:65% XNOR:187%	NOT:134% OR:223% AND:82% NOR:33% NAND:134% XOR:83% XNOR:223%
Transmission's Amplifying	OR gate, NAND gate, and XNOR gate	OR gate, AND gate, NAND gate, XOR gate and XNOR gat	NOT gate, OR gate, NAND gate, XNOR gate
The program used in the simulation	FEM-2D	FEM-2D	FEM-2D
Performance measured	Transmission and contrast ratio	Transmission and contrast ratio	Transmission and contrast ratio and modulation depth
Threshold of transmission	25%	25%	25%

V. CONCLUSION

In this paper, small-dimensional design (300 nm × 300 nm) was proposed. The proposed design capable of implementing seven logic gates (NOT, AND, OR, NAND, NOR, XOR, XNOR) using (2D-FEM) with maximum transmission 134% in NOT gate, 223% in OR gate, 134% in NAND gate and 223% in XNOR gate where the design is optimum based on modulation depth equation. the proposed design was created by (IMI). The gates were implemented at the wavelength of 1550 nm. The mechanism of the gate's work depends on the characteristic of the coupling between the nanoring and the strips. We can implement each gate by changing the position of the ports, the state of the ports and the angle of the transmission light. The design efficiency and performance of the gates were measured by three criteria: transmission, contrast ratio and modulation depth. The proposed transmission threshold is a criterion for distinguishing between OFF and ON state in the output ports. Finally, the proposed design contributes in building nanocircuits for optical signal processing and integrated photonic circuits.

REFERENCES

[1] S. H. Abdulnabi and M. N. Abbas, "Design an all-optical combinational logic circuits based on nano-ring insulator-metal-insulator plasmonic waveguides," *Photonics*, vol. 6, no. 1, 2019, doi: 10.3390/PHOTONICS6010030.

[2] T. S. M. H. F. Fakhruldeen and T. S. Mansour, "All-optical NoT Gate Based on Nanoring Silver-Air Plasmonic Waveguide," *Int. J. Eng. Technol. vol*, vol. 7, pp. 2818–2821, 2018.

[3] S. H. Abdulnabi, "All-optical logic gates based on nanoring insulator–metal–insulator plasmonic waveguides at optical communications band," *J. Nanophotonics*, vol. 13, no. 01, p. 1, 2019, doi: 10.1117/1.jnp.13.016009.

[4] A. Kotb and C. Guo, "All-optical multifunctional AND, NOR, and XNOR logic gates using semiconductor optical amplifiers," *Phys. Scr.*, vol. 95, no. 8, p. 85506, 2020.

[5] X. Mei, X. G. Huang, and T. Jin, "A sub-wavelength electro-optic switch based on plasmonic T-shaped waveguide," *Plasmonics*, vol. 6, no. 4, pp. 613–618, 2011.

[6] X. Peng, H. Li, C. Wu, G. Cao, and Z. Liu, "Research on transmission characteristics of aperture-coupled square-ring resonator based filter," *Opt. Commun.*, vol. 294, pp. 368–371, 2013.

[7] E. Ozbay, "Plasmonics: merging photonics and electronics at nanoscale dimensions," *Science (80-.).*, vol. 311, no. 5758, pp. 189–193, 2006.

[8] Y. Guo *et al.*, "Transmission characteristics of the aperture-coupled rectangular resonators based on metal–insulator–metal waveguides," *Opt. Commun.*, vol. 300, pp. 277–281, 2013.

[9] J. Chen, Z. Li, M. Lei, X. Fu, J. Xiao, and Q. Gong, "Plasmonic Y-splitters of high wavelength resolution based on strongly coupled-resonator effects," *Plasmonics*, vol. 7, no. 3, pp. 441–445, 2012.

[10] Z. Lu and W. Zhao, "Nanoscale electro-optic modulators

based on graphene-slot waveguides," *JOSA B*, vol. 29, no. 6, pp. 1490–1496, 2012.

[11]   J. Tao, Q. J. Wang, and X. G. Huang, "All-optical plasmonic switches based on coupled nano-disk cavity structures containing nonlinear material," *Plasmonics*, vol. 6, no. 4, pp. 753–759, 2011.

[12]   N. Nozhat and N. Granpayeh, "All-optical nonlinear plasmonic ring resonator switches," *J. Mod. Opt.*, vol. 61, no. 20, pp. 1690–1695, 2014.

[13]   Y. Liu, F. Qin, Z.-M. Meng, F. Zhou, Q.-H. Mao, and Z.-Y. Li, "All-optical logic gates based on two-dimensional low-refractive-index nonlinear photonic crystal slabs," *Opt. Express*, vol. 19, no. 3, pp. 1945–1953, 2011.

[14]   I. S. Maksymov, "Optical switching and logic gates with hybrid plasmonic–photonic crystal nanobeam cavities," *Phys. Lett. A*, vol. 375, no. 5, pp. 918–921, 2011.

[15]   Y.-D. Wu, Y.-T. Hsueh, and T.-T. Shih, "Novel All-optical Logic Gates Based on Microring Metal-insulator-metal Plasmonic Waveguides.," 2013.

[16]   A. Dolatabady and N. Granpayeh, "All-optical logic gates in plasmonic metal–insulator–metal nanowaveguide with slot cavity resonator," *J. Nanophotonics*, vol. 11, no. 2, p. 26001, 2017.

[17]   A. Dolatabady and N. Granpayeh, "All optical logic gates based on two dimensional plasmonic waveguides with nanodisk resonators," *J. Opt. Soc. Korea*, vol. 16, no. 4, pp. 432–442, 2012.

[18]   N. Nozhat and N. Granpayeh, "All-optical logic gates based on nonlinear plasmonic ring resonators," *Appl. Opt.*, vol. 54, no. 26, pp. 7944–7948, 2015.

[19]   H. K. Al-Musawi, A. K. Al-Janabi, S. A. W. Al-abassi, N. A. H. A. Abusiba, and N. A. H. Q. Al-Fatlawi, "Plasmonic logic gates based on dielectric-metal-dielectric design with two optical communication bands," *Optik (Stuttg).*, vol. 223, no. June, p. 165416, 2020, doi: 10.1016/j.ijleo.2020.165416.

[20]   R. Kékesi, "Étude expérimentale de cristaux magnéto photoniques 3D réalisés sous forme d'opales inversés par une matrice de silice dopée en nanoparticules magnétiques," Ph.D. dissertation, Dept. Sci. Eng., Jean Monnet Univ, Saint Etienne, FRA, 2011.

[21]   S. A. Maier, *Plasmonics: fundamentals and applications*. Springer Science & Business Media, 2007.

[22]   E. A. Freeman and G. G. Moisen, "A comparison of the performance of threshold criteria for binary classification in terms of predicted prevalence and kappa," *Ecol. Modell.*, vol. 217, no. 1–2, pp. 48–58, 2008.

[23]   M. N. Abbas and S. H. Abdulnabi, "Plasmonic reversible logic gates," *J. Nanophotonics*, vol. 14, no. 01, p. 1, 2020, doi: 10.1117/1.jnp.14.016003.

[24]   M. Yarahmadi, M. K. Moravvej-Farshi, and L. Yousefi, "Subwavelength graphene-based plasmonic THz switches and logic gates," *IEEE Trans. Terahertz Sci. Technol.*, vol. 5, no. 5, pp. 725–731, 2015.

[25]   M. H. Rezaei, A. Zarifkar, M. Miri, and A. Alighanbari, "Design of a high-efficient and ultra-compact full-adder based on graphene-plasmonic structure," *Superlattices Microstruct.*, vol. 129, pp. 139–145, 2019.

[26]   D. Choi, C. K. Shin, D. Yoon, D. S. Chung, Y. W. Jin, and L. P. Lee, "Plasmonic optical interference," *Nano Lett.*, vol. 14, no. 6, pp. 3374–3381, 2014.