Assessment of 50%-Propagation-Delay for Cascaded PCB Non-Linear Interconnect Lines for the High-Rate Signal Integrity Analysis

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Abstract

This paper is a special issue from the work presented in the *Advanced Electromagnetics Symposium 2012* (*AES'12*) which presents an enlarged study about the 50-% propagation-time assessment of cascaded transmission lines (TLs). First and foremost, the accurate modeling and measurement technique of signal integrity (SI) for high-rate microelectronic interconnection is recalled. This model is based on the reduced transfer function extracted from the electromagnetic (EM) behavior of the interconnect line RLCG-parameters. So, the transfer function established takes into account both the frequency dispersion effects and the different propagation modes. In addition, the transfer function includes also the load and source impedance effects. Then, the SI analysis is proposed for high-speed digital signals through the developed model. To validate the model understudy, a prototype of microstrip interconnection with $w = 500$ µm and length $d = 33$ mm was designed, simulated, fabricated and tested. Then, comparisons between the frequency and time domain results from the model and from measurements are performed. As expected, good agreement between the S-parameters form measurements and the model proposed is obtained from DC to 8 GHz. Furthermore, a de-embedding method enabling to cancel out the connectors and the probe effects are also presented. In addition, an innovative time-domain characterization is proposed in order to validate the concept with a 2.38 Gbit/s-input data signal. Afterwards, the 50-% propagation-time assessment problem is clearly exposed. Consequently an extracting theory of this propagation-time with first order RC-circuits is presented. Finally, to show the relevance of this calculation, propagation-time simulations and an application to signal integrity issues are offered.

1. Introduction

Over the last 50 years, the tremendous growth of the microelectronics industry has lead to an incessant increase of operating frequencies and integration scale densities of the chips and the electronic systems [1]. The combination of the functional diversification ("More than Moore") and the integration technologies ("More Moore") lead to new EMC challenges in order to make coexisting these micro-systems in restricted environments [1-2]. This arrangement of technologies is the worthwhile and strategic work to target in order to obtain a high value system [2-4]. In addition to this constant increase in density, since the digital systems reach very high data rates, the fidelity of these RF-digital signals must be taken into account by designers [3-6], [11]. In order to preserve the acceptable functioning of modern high speed digital electronics, since the early 1990s, critical requirements on the signal integrity (SI) were established [3], [5-6]. It is widespread that all electronic products have the same configuration, there are drivers that outputting signals to receivers through the interconnects [6]. This statement illustrates that the effects of interconnection lines cannot be neglected [7-8], for integrated circuits (ICs) [9] and PCBs [10-11].

Subsequently, one of the most important degradations in such systems is linked to the interconnection modeling for high-speed applications [1-3], [6], [12]. For this reason, more and more accurate interconnection network models are necessary to balance correctly the signals at different stage of the electronic boards [10-12]. A fast and accurate modeling of PCB TLs (Printed Circuit Boards Transmission Lines) for high-rate digital-mixed signal interconnects has been recently performed [13-14]. Whereas PCBs or TLs are well-known since the early of 1980s [15], some improvements seem to be still required [11] for the better understanding of the physical behavior [16] and the signal integrity forecasting for modern applications [17-22]. Indeed, facing to the widespread microwave theory, the PCB interconnects require faster and more accurate broadband models [18] and measurement techniques [23]. Therefore this field of investigation is extremely attractive, in particular for differential TLs or multilayer TLs [17] and time-domain analysis [24-25]. Undeniably, over the last five years many enhancements about the knowledge of TLs behavior have been highlighted [16-26]. Despite this technical progress, a major issue is inherent to the time-

domain prediction [27] and the calibration process [23]. In fact, the de-embedding technique is the critical point in order to accomplish a good agreement with the models [28]. Consequently, the ABCD matrix is one parameter which allows one to explore this bottleneck [17], [29], particularly for estimating the transient responses [25-28]. This statement motivates us to develop simpler and faster models to forecast the transient responses for digital interconnection lines on PCBs to help designers for high-speed applications [13-14], [30]. Moreover, as exposed above, interconnects play an important role in designing modern electronic and microelectronic systems. So the degradations engendered by these interconnects can be partially reduced by the repeaters insertion [31] or completely reduced using the NGD concept as recently introduced [32-35].

Furthermore, since the early 1990s, it has been evidenced that the interconnect delays of high speed digital IC dominate widely gate delays [1]. In telecommunication area, these technological issues can be sources of distortions, asynchronous effects of the transmitted analog signals and erroneous symbols of numerical data. In order to deal with this difficulty, intensive researches for the enhancement of on-chip interconnects have been conducted [36-41]. To estimate the interconnect delay, the most popular method is based on the use of RC-models as introduced by Elmore in 1948 [42-54]. In that case, the propagation delay expression can be established only from the first order approximation of the system transfer function. The main advantage of this model lies on its simplicity and its possibility for fast delay estimation when considering sophisticated signal paths of integrated system. However, its drawback is its drastic high imprecision compared to other high order delay models. It was reported that Elmore model can involve to more than 30-% relative errors [55-57]. For this reason, more accurate approximated second order RLC model with closed form of delay times (propagation-, rise-/fall- and settling- time delays) were developed in [55-57]. Furthermore, as developed in [56-57], authors determine the step unit response of lumped RLC tree networks via second moments of the polynomial transfer function. Then, they deduce the basic characteristics of the transient response (over- or under-damped responses) and propose also the specific expression of 2nd order propagation delay. The main advantage of this 2nd order delay model is the fact that it enables to investigate the signal delay with good accuracy even for non-monotone time-domain responses. Furthermore, compared to SPICE-computation, this model can guarantee relative errors lower than 5%.

Propagation delay T_p is one of the fundamental important parameters for the evaluation of the numerical-analogue high-speed system characteristics. This delay plays an important role for the interconnect structure optimization [58]. In fact, the propagation delay can limit the speed or the rate f_{max} of the operating data as explained by the relation:

$$f_{\max} < \frac{1}{T_p}. \quad (1)$$

Till now, the most popular model for estimating the propagation delay was established by Elmore [9], [59-61]. To overcome this technical limitation, in this paper, a modeling method of cascaded system propagation delay is established. To gain a better understanding, this paper is structured in five sections, with the first third sections from the works presented in [70]. *Section 2* offers the theoretical approach of extracting the RLCG model of microstrip lines. First of all, the characteristic impedance and the propagation constant including frequency dispersion and propagation modes effects are established in function of the geometrical and physical properties of the interconnect line. Then the overall voltage transfer function for an interconnected electronic system is extracted, including source impedance and load impedance effects. In order to demonstrate the relevance of this model, *Section 3* presents frequency- and time-domain investigations performed with an original "omega" shape interconnect line. The validation process will be presented by considering frequency-/time-domains measurements achieved with the innovative improved TDR / TDT (Time-Domain Reflectometry / Time-Domain Transmissiometry) equipment introduced in [62-69]. This allows one to illustrate the evidence of the effects of connectors and the de-embedding process consequences. Subsequently, the trouble in evaluating properly the propagation time is exposed, thus a theory of propagation-time extraction is presented in *Section 4*. This theoretical study is followed by verification results reported in *Section 5*. Finally, the last section draws the conclusion of the paper.

2. Theoretical approach

This section is structured in two paragraphs. First, we recall the characterization theory of microstrip lines including the extraction method of per unit length parameters *R*, *L*, *C* and *G*. Then, knowing the RLCG-model of the line, the analytical expressions of the transfer function and the access impedances of the line are introduced in the second paragraph.

2.1. Electromagnetic parameters extraction of a single transmission line (TL)

One considers a microstrip TL, of length *d*, with EM (Electromagnetic) parameters propagation constant $\gamma(\omega) = \alpha(\omega) + j\beta(\omega)$ (with $j = \sqrt{-1}$) and characteristic impedance, $Z_c(\omega)$, defined from physical properties (permittivity ε_r, dielectric loss tangent $tan\delta$, metal resistivity ρ…) and geometrical properties (width *w*, metallization thickness *t* and substrate height *h*) in function of the frequency as sketched on Figure 1.

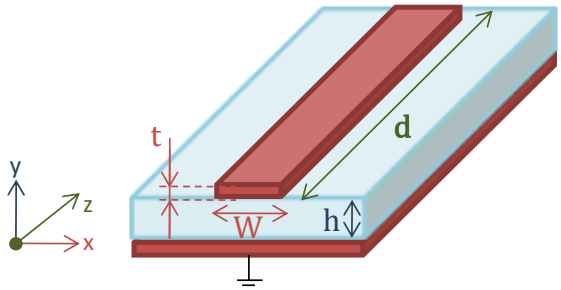

Figure 1: Geometrical representation of a microstrip TL.

According to the microwave theory [15], the well-known microstrip line synthesis and analysis relations [20], which are used in the EMDS (Electromagnetic Design System) environment of ADS (Advanced Design System) simulation tool, permit to extract the characteristic impedance:

$$Z_c = \frac{\eta_0}{2\pi\sqrt{\varepsilon_{eff}}} \ln\left[\frac{h \cdot F(w/h)}{w} + \sqrt{1+\frac{4h^2}{w^2}}\right], \quad (2)$$

where

$$F(w/h) = 6 + (2\pi - 6)\cdot \exp\left[-\left(\frac{30.66h}{w}\right)^{0.7528}\right], \quad (3)$$

η_0 is the air impedance and ε_{eff} is the effective relative permittivity of the medium. In order to reach a better accuracy, this model must be valid a wide frequency bandwidth. For this reason, frequency dispersion effects can be taken into account if the characteristic impedance is considered as follow:

$$Z_c(f) = Z_c \cdot \sqrt{\frac{\varepsilon_{eff}}{\varepsilon_r(f)}} \cdot \frac{\varepsilon_r(f)-1}{\varepsilon_{eff}-1}, \quad (4)$$

with

$$\varepsilon_r(f) = \varepsilon_r - \frac{\varepsilon_r - \varepsilon_{eff}}{1+g\cdot\left(f/f_p\right)^2}, \quad (5)$$

$$g = \frac{\pi^2}{12}\cdot\frac{\varepsilon_r - 1}{\varepsilon_{eff}}\cdot\sqrt{\frac{Z_c}{\eta_0}}, \quad (6)$$

$$f_p = \frac{Z_c}{2\cdot\mu_0\cdot h}. \quad (7)$$

And by replacing $u = w/h$, ε_{eff} is given by:

$$\varepsilon_{eff} = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\cdot\left(1+\frac{10}{u}\right)^{-a(u)b(\varepsilon_r)}, \quad (8)$$

$$a(u) = 1 + \frac{1}{49}\ln\left(\frac{u^4 + \left(u/52\right)^2}{u^4+0.432}\right) + \frac{1}{18.7}\ln\left(1+\left(\frac{u}{18.1}\right)^3\right), \quad (9)$$

$$b(\varepsilon_r) = 0.564\cdot\left(\frac{\varepsilon_r - 0.9}{\varepsilon_r + 3}\right)^{0.053}. \quad (10)$$

In this reminder, it is worthy of note to mention that a particular point of attention should be considered regarding the effective width w_{eff} of the structure. Indeed, a conformal transformation should be performed with respect of the value of u [15] as follow:

$$w_{eff} = \begin{cases} w + \frac{1.25}{\pi}\cdot\left(1+\ln\left(\frac{2h}{t}\right)\right), & if \quad u < \frac{1}{2\pi} \\ w + \frac{1.25}{\pi}\cdot\left(1+\ln\left(\frac{4\pi w}{t}\right)\right), & if \quad u \geq \frac{1}{2\pi} \end{cases}. \quad (11)$$

One also considers the propagation mode effects, hence the propagation constant in function of the frequency can be written, by denoting c the celerity, as:

$$\gamma(f) = \alpha_c(f) + \alpha_d(f) + j\frac{2\pi f}{c}\sqrt{\varepsilon_r(f)}, \quad (12)$$

includes the metallic conductor and the dielectric losses respectively given by:

$$\alpha_c(f) = 1.38\cdot\left\{1+\frac{h}{w_{eff}}\cdot\left[1+\frac{1}{\pi}\cdot\ln\left(\frac{2h}{t}\right)\right]\right\}\cdot\frac{R_s(f)}{h\cdot Z_c(f)}\cdot\frac{32-\left(\frac{w}{h}\right)^2}{32+\left(\frac{w}{h}\right)^2} \quad (13)$$

$$\alpha_d(f) = 27.3\cdot\frac{\varepsilon_r}{\varepsilon_r-1}\cdot\frac{\varepsilon_{eff}-1}{\sqrt{\varepsilon_{eff}}}\cdot\frac{\tan(\delta)}{\frac{2\pi f}{c}} \quad (14)$$

with

$$R_s(f) = \sqrt{\pi\cdot f\cdot\mu_0\cdot\rho} \quad (15)$$

For the calculation including the radiating losses, more explicit analytical expressions of the propagation constant real part or the per unit length losses constant $\alpha(f)$ is presented in [15-16]. Since the RLCG model is associated

with the propagation constant and the characteristic impedance of the transmission line as:

$$\gamma(j\omega)\cdot d = \sqrt{R+j\omega L}\times\sqrt{G+j\omega C}\,, \tag{16}$$

$$Z_c(j\omega) = \frac{\sqrt{R+j\omega L}}{\sqrt{G+j\omega C}}\,, \tag{17}$$

one can also extract straightforwardly the RLCG parameters of any interconnect lines by substituting [13]:

$$R(f) = \Re\{\gamma(f)\cdot Z_c(f)\}\cdot d\,, \tag{18}$$

$$L(f) = \frac{\Im\{\gamma(f)\cdot Z_c(f)\}}{\omega}\cdot d\,, \tag{19}$$

$$C(f) = \frac{\Im\left\{\dfrac{\gamma(f)}{Z_c(f)}\right\}}{\omega}\cdot d\,, \tag{20}$$

$$G(f) = \Re\left\{\frac{\gamma(f)}{Z_c(f)}\right\}\cdot d\,, \tag{21}$$

2.2. Voltage transfer function determination of a TL

Getting an accurate voltage transfer function (VTF) of an interconnection line yields to determine the domain of validity of the presented equations (2) to (15). The simpler approximation that one can provide is to bound the upper frequency, f_{max}, in function of the substrate height [11] as:

$$f_{max} \le \frac{c}{10\cdot h\cdot\sqrt{\varepsilon_r}}\,. \tag{22}$$

In this case one can assume that the TL offers quasi-TEM solution for propagating. Hence, the TL is characterized by the following ABCD matrix [15]:

$$[M_{TL}] = \begin{bmatrix} \cosh(\gamma(\omega)\cdot d) & Z_c(\omega)\cdot\sinh(\gamma(\omega)\cdot d) \\ \dfrac{\sinh(\gamma(\omega)\cdot d)}{Z_c(\omega)} & \cosh(\gamma(\omega)\cdot d) \end{bmatrix} \tag{23}$$

One proposes the real electronic system like two gates connected together through a PCB interconnection line, as depicted on Figure 2 for evaluating the SI.

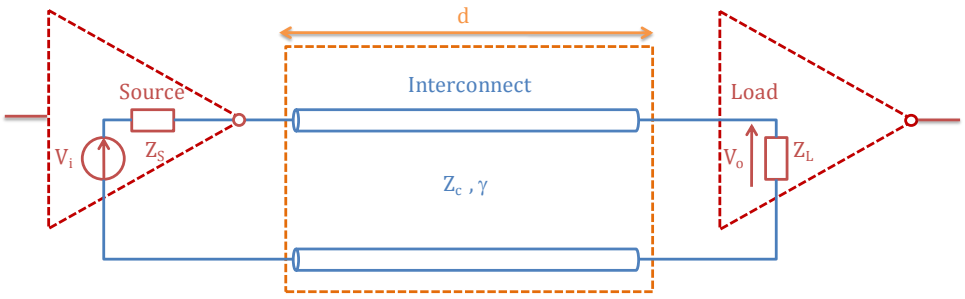

Figure 2: Circuit diagram representing interconnect line driven by source gate with impedance Z_S and loaded by input impedance Z_L.

Since, the SI assessment is based on the equivalent analog bandwidth of a considered input signal. Consequently, the RLCG-interconnection VTF should present the same bandwidth, this becomes challenging especially for high-rate signal due to important rise times [13]. Indeed, the equivalent frequency bandwidth *BW* for a trapezoidal signal is related to the 10% to 90% rise time, $t_{r\,90\text{-}10}$, as:

$$BW \approx \frac{0.35}{t_{r90\text{–}10}}\,. \tag{24}$$

As a result, the frequency-domain of validity of the VTF must satisfy relations (22) and (24). So, the overall TL transfer matrix M_{ij} including the source Z_S, and load Z_L, impedances within the frequency band of interest is given by the matrix product expressed in (25). Afterwards, SI parameters can be established straightforwardly from the impedance matrix and the transient responses [14].

$$\begin{bmatrix} M_{11}(\omega) & M_{12}(\omega) \\ M_{21}(\omega) & M_{22}(\omega) \end{bmatrix} = \begin{bmatrix} 1 & Z_S(\omega) \\ 0 & 1 \end{bmatrix} \times [M_{TL}] \times \begin{bmatrix} 1 & 0 \\ \dfrac{1}{Z_L(\omega)} & 1 \end{bmatrix} \tag{25}$$

In fact, the VTF denoted $H(j\omega)$, the input impedance $Z_{in}(j\omega)$, the output impedance $Z_{out}(j\omega)$ and the transfer impedance $Z_T(j\omega)$ of the considered system of the Figure 2 are respectively summarized in Table 1:

Table 1: Summary of extracted frequency-domain SI parameters.

SI Element	Expression
$H(j\omega)$	$\dfrac{1}{\left[\dfrac{Z_c(j\omega)}{Z_L(j\omega)}+\dfrac{Z_S(j\omega)}{Z_c(j\omega)}\right]\cdot\sinh\left(\gamma(j\omega)\cdot d\right)+\left[1+\dfrac{Z_S(j\omega)}{Z_L(j\omega)}\right]\cdot\cosh\left(\gamma(j\omega)\cdot d\right)}$
$Z_{in}(j\omega)$	$\dfrac{\left(Z_c^2(j\omega)+Z_L(j\omega)\cdot Z_S(j\omega)\right)\cdot\sinh\left(\gamma(j\omega)\cdot d\right)+Z_c(j\omega)\cdot\left(Z_L(j\omega)+Z_S(j\omega)\right)\cdot\cosh\left(\gamma(j\omega)\cdot d\right)}{Z_L(j\omega)\cdot\sinh\left(\gamma(j\omega)\cdot d\right)+Z_c(j\omega)\cdot\cosh\left(\gamma(j\omega)\cdot d\right)}$
$Z_{out}(j\omega)$	$\dfrac{Z_c(j\omega)\cdot Z_L(j\omega)\cdot\cosh\left(\gamma(j\omega)\cdot d\right)}{Z_L(j\omega)\cdot\sinh\left(\gamma(j\omega)\cdot d\right)+Z_c(j\omega)\cdot\cosh\left(\gamma(j\omega)\cdot d\right)}$
$Z_T(j\omega)$	$\dfrac{Z_c(j\omega)\cdot Z_L(j\omega)}{Z_L(j\omega)\cdot\sinh\left(\gamma(j\omega)\cdot d\right)+Z_c(j\omega)\cdot\cosh\left(\gamma(j\omega)\cdot d\right)}$

3. Frequency- and time-domain investigations

As concrete proof-of-concept, the "**omega**" shape microstrip interconnect displayed in Figure 3 was considered and characterized by the TDR/TDT techniques. The equipment used in this experiment applies de-noising algorithms [68] on all the 40-GHz instantaneous bandwidth TDR/TDT traces. This allows performing straightforwardly and accurately the de-embedding of the SMA connectors in [62]. The interconnect-under-test (IUT) presents a width $w = 0.5$ mm, and a length $d = 32.944$ mm printed on the FR4-epoxy substrate, of height $h = 1.6$ mm, having relative permittivity $\varepsilon_r = 4.4$. Figure 4 represents the schematic diagram of the circuit tested by considering an interconnection with complex form. This interconnect corresponds to the length of PCB interconnections for mixed-circuit as PLL or clock distribution [69].

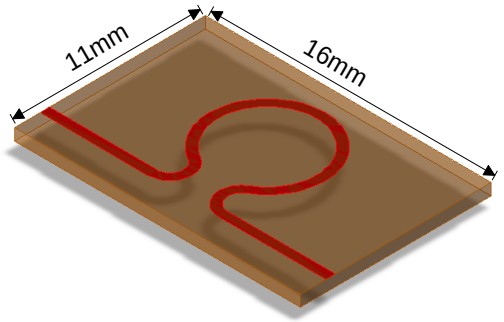

Figure 3: Interconnect microstrip line under test.

EM full-wave simulations of the 3-D structure represented by the black box of Figure 4 were performed in the EM design system environment, "Momentum", of ADS microwave/electronic tool. This IUT was also modeled with the method proposed in *Section 2*.

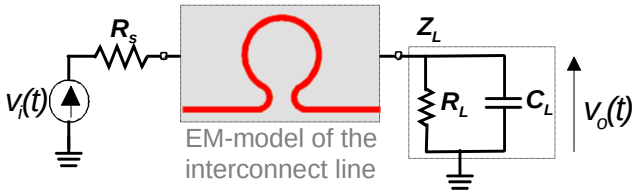

Figure 4: Schematic diagram used for the EM/circuit co-test.

3.1. Assessing the de-embedding effects

At present time, the de-embedding process of the SPARQ is under consideration. First, the IUT is characterized with using a VNA (Vector Network Analyzer) within the frequency-domain from 100 kHz to 8.5 GHz. The calibration was made in SOLT including port extension (open and short) of the universal test fixture for PCB, as presented by the photograph in Figure 5.

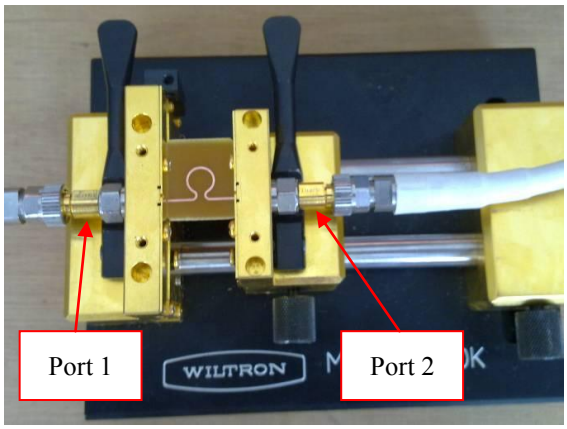

Figure 5: Universal test fixture used for the IUT characterization

Afterwards, comparison was made with the SPARQ measurement in the time-domain for de-embedding ports 1 and 2. The ports are de-embedded via an algorithm that uses S-parameter measurement, and thus the S-parameters for these components must be known prior to the time of measurement. Hence, SPARQ calculates first the gated-port's S-parameters and then uses them in de-embedding connectors [62, 63]. Table 2 proposes the comparison between the time delays engendered by the connectors obtained from VNA with port extension (SOLT calibration) and TDR/TDT measurement performed with the SPARQ. Then, the S-parameters were also obtained with the SPARQ measurement within the time-domain including the "*gating*" process for de-embedding connectors [62-63], [68]. Hereafter, magnitude of the S_{11} (a), S_{21} (b) and phase of the S_{21} (c) are offered in Figure 6, from the EM simulation (black continuous curves), the proposed model (blue dashed curves), the VNA measurement (green dashed curves) and the SPARQ measurement (red continuous curves).

Table 2: Port extension for de-embedding connectors.

Port	VNA	SPARQ
Port 1	91.4 ps	90 ps
Port 2	90.5 ps	89 ps

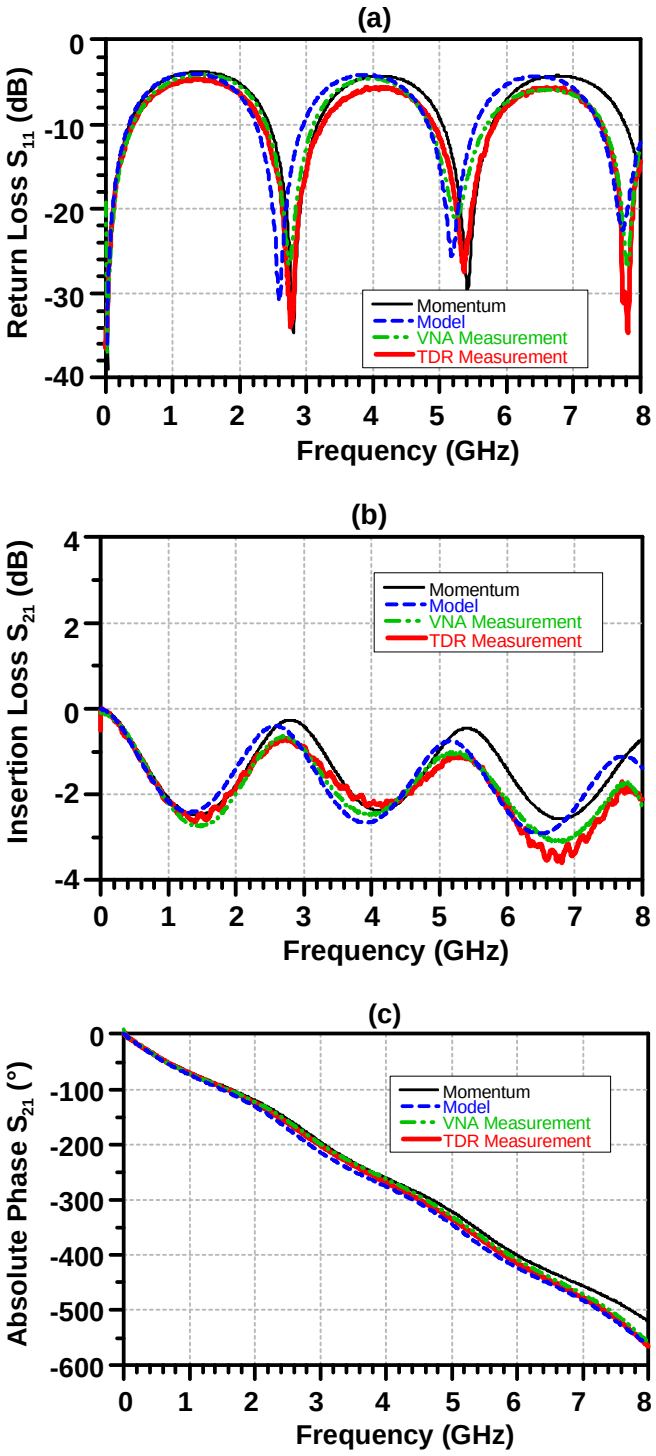

Figure 6: Comparisons of S_{11}-amplitude (a) and S_{21}-amplitude (b) and S_{21}-phase (c) from the EM model obtained from momentum, the developed model, the VNA measurement and the TDR/TDT measurement.

3.2. Application to the signal integrity forecasting

Using the SI Studio feature, a noisy digital-mixed input v_{in} with 2.38-Gbit/s rate and 42-ps rise-time was simulated. Then, in order to emulate SI parameters degradation by considering $R_s = 20\ \Omega$, $R_L = 500\ \Omega$ and $C_L = 2$ pF, the Virtual-Probing was performed [44].

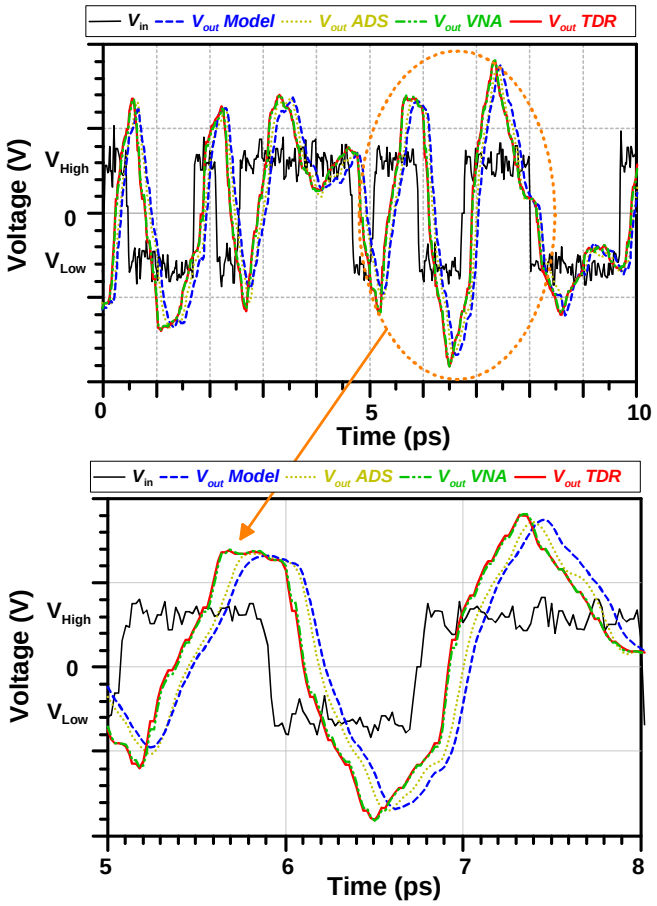

Figure 7: Comparison between the different techniques for a NRZ noisy 2.38 Gpbs input signal.

Indeed, the SI Studio capability allows one to forecast the transient response of the system as shown by Figure 7. In addition, comparisons were made between the transient responses obtained from SI Studio with the VNA (green dashed curves) and the SPARQ measurements (red continuous curves) and between the simulations obtained from the developed model (blue dashed curves) and from ADS (ocher dashed curves). An excellent correlation was found between the VNA results and the SPARQ measurements that give evidence of the de-embedding method efficiency. In addition a very good agreement is established between the developed theoretical model and the measurements.

A major issue in signal integrity is inherent to the accurate assessment of the 50%-propagation time. Indeed, this latter is linked to the group delay of the system which evolves considerably in a wide frequency band. To manage this problem some complicated numerical approaches exist, but this difficulty increases when one considers cascaded transmission lines.

4. Theoretical extraction of the propagation-time

For the complex structures composed of different systems in cascade as the circuit network depicted in Figure 8, the sum of the Elmore propagation delay is generally used [44-47]:

$$T_p = \sum_{k=1}^{n} R_k \cdot C_k \ . \qquad (26)$$

But this relation is susceptible to generate a relative error higher than 35 % [50][56-57].

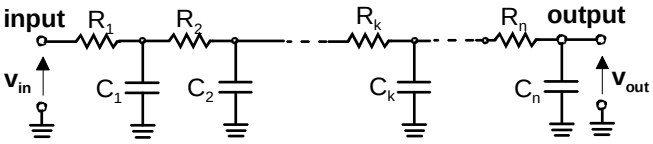

Figure 8: RC-network composed of n-cells in cascade.

It is well-known that the voltage transfer function (VTF) of linear circuits can be expressed as:

$$G_n(s) = \frac{1}{1 + \sum_{k=1}^{n} a_k \cdot s^k}, \qquad (27)$$

In this case, the Elmore model propagation delay induced by this system is written as [42]:

$$T_{pElmore} = a_1 \ . \qquad (28)$$

As argued above this expression present a very high inaccuracy [50][56-57], so, in the next paragraphs, we will develop mathematical expressions enabling to realize more precise value of propagation delay associated to more generalized systems.

4.1. Transfer function modeling of cascaded RC-network

This subsection focus is on the modeling of the RC network introduced in Figure 8 for $k = \{1 \ldots n\}$. Being given that this lumped network is a linear circuit, its transfer equation should be governed also by a linear differential equation. This finding leads us to suppose that the elements of the ABCD-matrix:

$$\left[T_n(s)\right] = \begin{bmatrix} T_{11,n}(s) & T_{12,n}(s) \\ T_{21,n}(s) & T_{22,n}(s) \end{bmatrix}, \tag{29}$$

as polynomial expressions having real coefficients. So that, the two first elements $T_{11,n}(s) = A_n(s)$ and $T_{12,n}(s) = B_n(s)$ can be written as:

$$A_n(s) = 1 + \sum_{k=1}^{n} a_k \cdot s^k , \tag{30}$$

$$B_n(s) = \sum_{l=0}^{n} b_k \cdot s^k , \tag{31}$$

with a_k and b_k are real coefficients. For n = 1, one takes the initial value:

$$A_1(s) = 1 + R_1 \cdot C_1 \cdot s , \tag{32}$$

$$B_1(s) = R_1 . \tag{33}$$

For $k = \{1,\ldots,n\}$, The whole ABCD-matrix can be determined with the successive matrix product [71]:

$$\left[T_{k+1}(s)\right] = \left[T_k(s)\right] \cdot \begin{bmatrix} 1 + R_{k+1} \cdot C_{k+1} \cdot s & R_{k+1} \\ C_{k+1} \cdot s & 1 \end{bmatrix}, \tag{34}$$

with

$$\left[T_1(s)\right] = \begin{bmatrix} 1 + R_1 \cdot C_1 \cdot s & R_1 \\ C_1 \cdot s & 1 \end{bmatrix}. \tag{35}$$

The coefficients a_k and b_k can be determined easily via substitutions of expressions (30) and (31) into relation (34). This yields the following iterative relations enabling the calculation of three first coefficients corresponding to $a_k(l)$ and $b_k(l)$ for $l = \{0, 1, 2\}$. So, by identification of $T_{11,n}(s)$-coefficients, the following expressions are established [71]:

$$a_{k+1}(1) = \begin{cases} R_1 \cdot C_1 & if \quad k = 0 \\ a_k(1) + C_k \cdot b_k(0) + R_k \cdot C_k & if \quad k \geq 1 \end{cases}, \tag{36}$$

$$a_{k+1}(2) = \begin{cases} 0 & if \quad k = 0 \\ a_k(2) + R_k \cdot C_k \cdot a_k(1) + C_k \cdot b_k(1) & if \quad k \geq 1 \end{cases}, \tag{37}$$

The same analysis applied to the $T_{12,n}(s)$ -coefficients permits to demonstrate the following expressions:

$$b_{k+1}(0) = \begin{cases} R_1 & if \quad k = 0 \\ b_k(0) + R_k & if \quad k \geq 1 \end{cases}, \tag{38}$$

$$b_{k+1}(1) = \begin{cases} 0 & if \quad k = 0 \\ b_k(1) + R_k \cdot a_k(1) & if \quad k \geq 1 \end{cases}, \tag{39}$$

$$b_{k+1}(2) = \begin{cases} 0 & if \quad k = 0 \\ R_k \cdot a_k(2) + b_k(2) & if \quad k \geq 1 \end{cases}. \tag{40}$$

By using this polynomial characteristic function, in the next section, we will evaluate the propagation delay for the high-order linear systems.

4.2. Propagation delay modeling of first order cascaded systems

For the better illustration, knowing the real constants τ_a and τ_b, one assigns the hereafter elementary transfer function:

$$G_a(s) = \frac{1}{1 + \tau_a \cdot s}, \tag{41}$$

and

$$G_b(s) = \frac{1}{1 + \tau_b \cdot s} . \tag{42}$$

For the sake of simplification, the following 50%-propagation delays are considered:

$$\begin{cases} T_{p\alpha} = \tau_a, T_{p\beta} = \tau_b & if \quad \tau_a < \tau_b \\ T_{p\beta} = \tau_a, T_{p\alpha} = \tau_b & if \quad \tau_b < \tau_a \end{cases}, \tag{43}$$

So that one denotes λ the real constant higher 1 given by:

$$\lambda = \frac{T_{p\beta}}{T_{p\alpha}} , \tag{44}$$

One demonstrates mathematically that if $\lambda \leq 4$, the 50%-propagation delay associated to the cascaded system with transfer function $G(s) = G_a(s) \cdot G_b(s)$ is defined as:

$$T_p = 0.41 \cdot T_{p\alpha} \left(e^{\sqrt{\lambda}} + \lambda \cdot e^{\frac{1}{\sqrt{\lambda}}} \right). \tag{45}$$

In the contrary case $\lambda > 4$, it is expressed as follows:

$$T_p = \frac{\lambda \cdot \ln\left(\frac{2 \cdot \lambda}{\lambda - 1}\right)}{\ln 2} \cdot T_{p\alpha} . \tag{46}$$

To verify the effectiveness of this theoretic concept, in the next section, validation results are proposed.

5. Application to the analysis of the SI issues

Up to certain frequency bandwidth, the microstrip interconnect circuit depicted in Figure 9 can be assumed as an RC-network cascaded. R_S and C_L represent respectively the source resistance and the load capacitance.

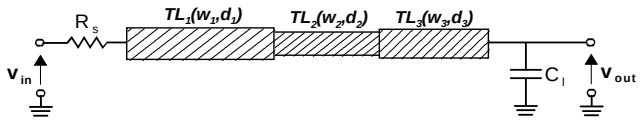

Figure 9: Microstrip lines in cascade.

Let us consider the structure as presented above having the characteristic summarized in Table 3 and depicted on Figure 10. The physical dimensions of the interconnections are printed on the FR4-substrate (relative permittivity $\varepsilon_r = 4.4$ and height $h = 500$ µm). By applying the modeling method introduced in [13] and [70] one evaluates the per unit length parameters at 7 GHz shown in Table 3.

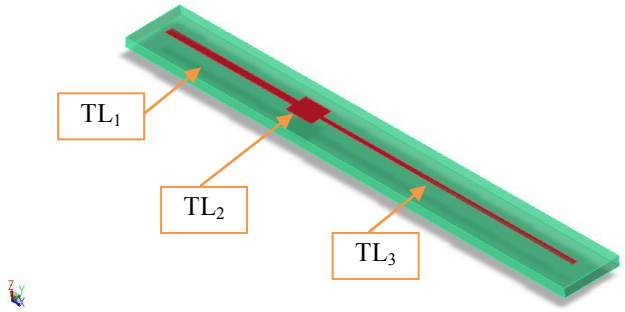

Figure 10: Microstrip lines in cascade understudy.

Table 3: Parameters of the interconnect microstrip line under consideration.

TL	w (mm)	d (mm)	R_U ($\Omega.m^{-1}$)	C_U ($pF.m^{-1}$)
TL_1	0.5	10	296.46	54.40
TL_2	1.5	2.0	203.04	83.96
TL_3	0.3	20	345.56	47.05

By considering each elementary interconnect lines by the following characteristic impedance:

$$Z_c(s) = \sqrt{R_u / (C_u \cdot s)}\ , \qquad (47)$$

and propagation constant:

$$\gamma(s) = \sqrt{R_u \cdot C_u \cdot s}\ , \qquad (48)$$

the corresponding m ABCD matrix of the m-th interconnect line, denoted $[TL_m]$, where here $m = \{1,2,3\}$, is given by:

$$[TL_m(s)] = \begin{bmatrix} \cosh(\gamma_m(s)\cdot d_m) & Z_{c_m}(s)\cdot\sinh(\gamma_m(s)\cdot d_m) \\ \dfrac{\sinh(\gamma_m(s)\cdot d_m)}{Z_{c_m}(s)} & \cosh(\gamma_m(s)\cdot d_m) \end{bmatrix}. \qquad (49)$$

By taking into consideration the maximum frequency bandwidth of a digital signal v_{in}, any transmission lines m can be modeled by N_m RC-circuits if N_m respects the following condition:

$$N_m \geq \frac{d_m \cdot f_{max} \cdot \sqrt{\varepsilon_{reff_m}}}{0.035 \cdot c}. \qquad (50)$$

Thus, in the presented case the ABCD matrix of each transmission line m will be given by:

$$[TL_m(s)] \approx \begin{bmatrix} 1 + \dfrac{R_u \cdot C_u \cdot s \cdot d_m}{N_m} & \dfrac{R_u \cdot d_m}{N_m} \\ \dfrac{C_u \cdot s \cdot d_m}{N_m} & 1 \end{bmatrix}^{N_m}. \qquad (51)$$

So the overall matrix denoted M_{TT}, of the whole system presented in Figure 9, can be considered as:

$$[M_{TT}(s)] \approx \begin{bmatrix} 1 & R_S \\ 0 & 1 \end{bmatrix} \times \left(\prod_{m=1}^{m=3} [TL_m(s)] \right) \times \begin{bmatrix} 1 & 0 \\ C_L \cdot s & 1 \end{bmatrix}. \qquad (52)$$

By using this relation, the two different length topologies of the structure presented in Figure 10 were studied. The number of cells characterizing each TL_m by considering a trapezoidal input signal having 50ps rise-time is given below by Table 4:

Table 4: Number of elementary cells for d_m length in the case 1 and in the case 2.

	Case 1		Case 2	
m	d_m (mm)	N_m	d_m (mm)	N_m
1	10	12	1.0	2
2	2.0	3	0.2	1
3	20	24	2.0	3

First, the VTF of the whole system was simulated using ADS with the microstrip TL model. By varying C_L = {0.5, 1.0, 2.0, 4.0} pF the magnitude (a) and the absolute phase (b) of the VTF is depicted on Figure 11 for case 1 and on Figure 12 for case 2. Then the transient responses were also simulated in the ADS environment by varying C_L for case 1 (Figure 13) and case 2 (Figure 14). Finally the 50%-propagation time calculated from the described model was compared with the Elmore one and the equivalent RC-model of the TLs in SPICE (Figure 15). Results, including relative errors, are summarized in Table 5 to Table 8.

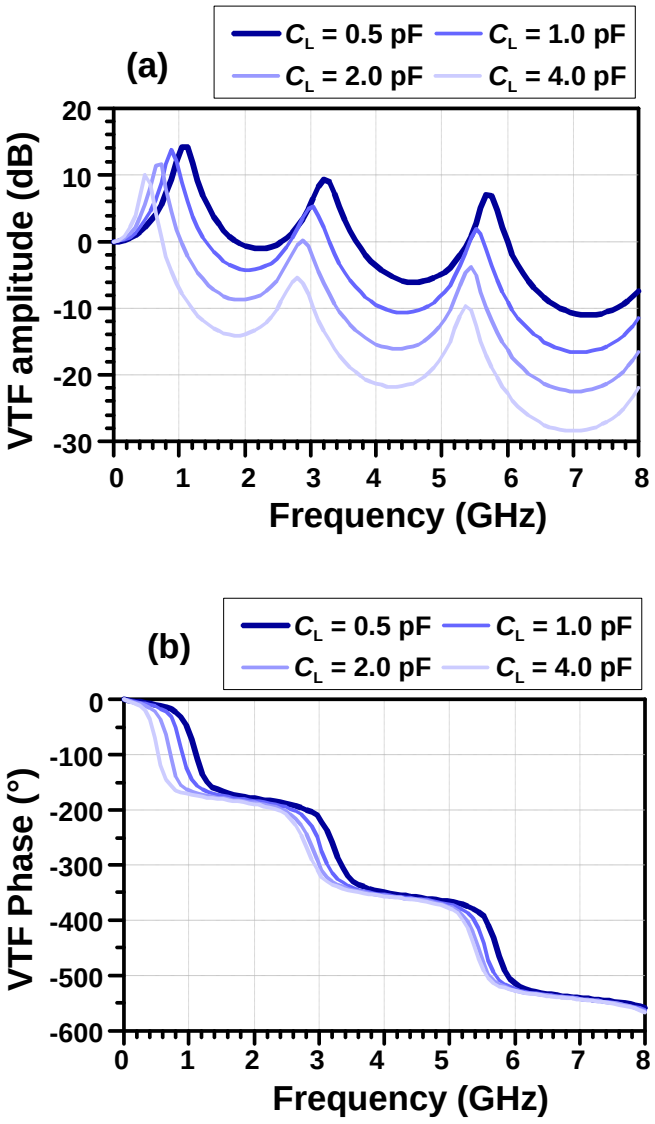

Figure 11: Frequency responses versus load C_L for the magnitude (a) and the phase (b) of the VTF for case 1.

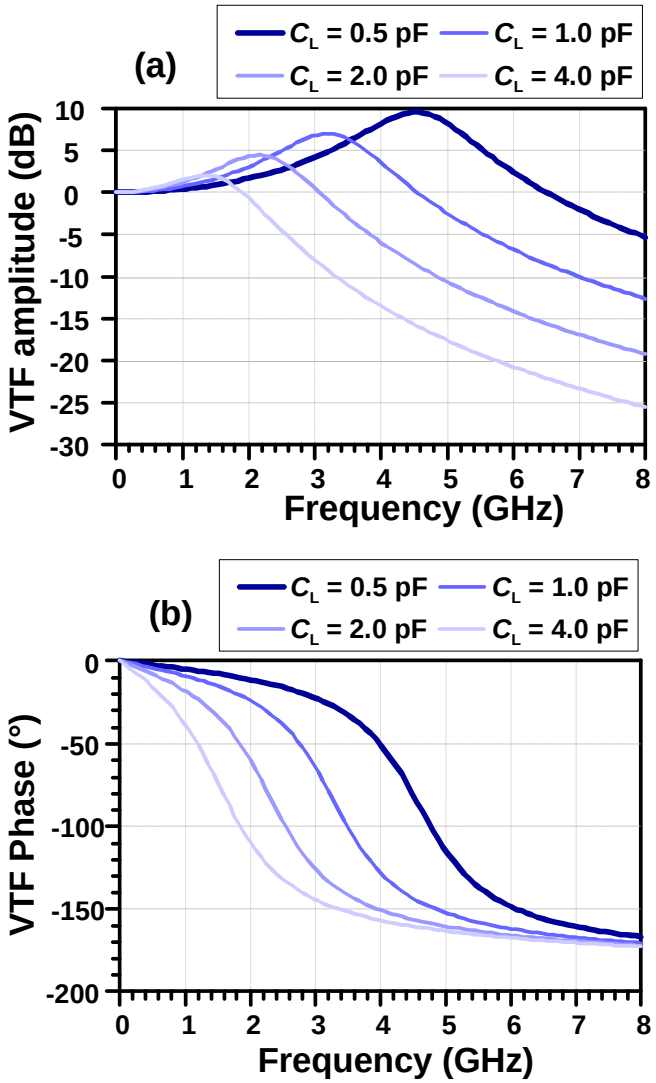

Figure 12: Frequency responses versus load C_L for the magnitude (a) and the phase (b) of the VTF for case 2.

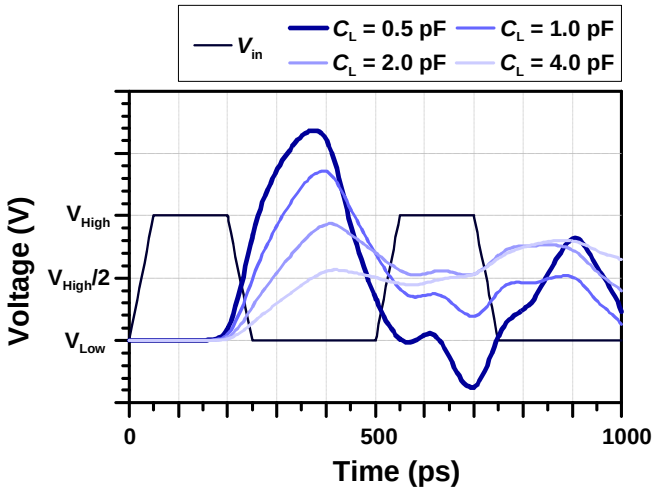

Figure 13: Transient responses versus load C_L for case 1.

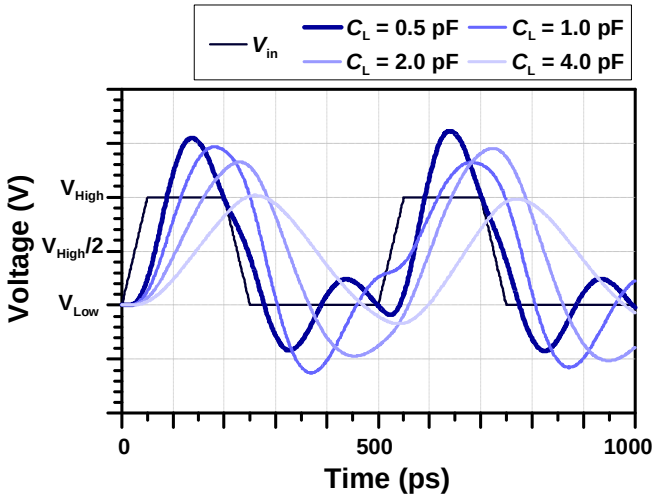

Figure 14: Transient responses versus load C_L for case 2.

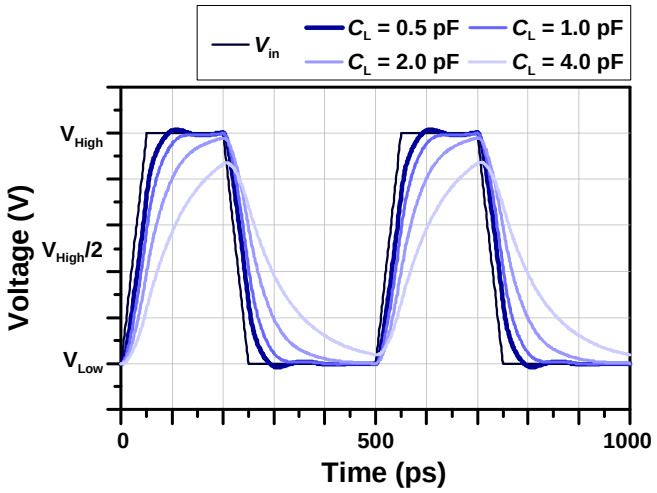

Figure 15: RC-SPICE Transient responses versus load C_L for case 2.

Table 5: Comparison of the 50%-propagation delay computed with SPICE and calculated with the proposed model the Elmore one versus load C_L for the case 1.

C_L (pF)	ADS 50%-T_p (ps)	SPICE RC-Circuits 50%-T_p (ps)	Model 50%-T_p (ps)	Elmore 50%-T_p (ps)
0.5	225.2	40.0	56.17	56.15
1.0	244.6	47.0	71.51	71.31
2.0	260.1	58.0	102.0	101.6
4.0	270.2	72.0	162.8	162.2

Table 6: Relative error between the 50%-propagation delay computed with the proposed model and the Elmore versus load C_L for the case 1.

C_L (pF)	Model Relative Error (%)	Elmore Relative Error (%)
0.5	74.9	75.0
1.0	70.7	70.8
2.0	60.7	60.9
4.0	39.7	39.9

Table 7: Comparison of the 50%-propagation delay computed with SPICE and calculated with the proposed model and the Elmore one versus load C_L for the case 2.

C_L (pF)	ADS 50%-T_p (ps)	SPICE RC-Circuits 50%-T_p (ps)	Model 50%-T_p (ps)	Elmore 50%-T_p (ps)
0.5	52.1	13.0	13.92	13.91
1.0	71.3	21.0	24.44	24.43
2.0	97.1	32.1	44.46	44.45
4.0	120.6	51.1	87.52	87.51

Table 8: Relative error between the 50%-propagation delay computed with the proposed model and the Elmore one versus load C_L for the case 2.

C_L (pF)	Model Relative Error (%)	Elmore Relative Error (%)
0.5	73.2	73.3
1.0	65.7	65.7
2.0	54.2	54.2
4.0	27.4	27.4

6. Conclusions

This paper reviews a modeling method of microstrip interconnections with reduced VTF. The theoretical analyses of the interconnections are recalled. Then, basic expressions of the VTF and access impedances including the driven gate and gate load are established. In order to validate the model established, a particular shape microstrip interconnect was characterized, designed and measured. Investigations both with frequency- and time-domain equipments were achieved in order to characterized PCB-interconnects. The de-embedding technique efficiency of the SPARQ Signal Integrity Network Analyzer was also exposed. The potential use for signal integrity forecasting was clearly shown. An excellent agreement was found between modern and complicate electronic simulation tools and the SI studio and Virtual-Probing environments from SPARQ measurements.

In addition, the interest of developed de-embedding technique can be applied to investigations microelectronic systems, as well bounding wires or lead frame effects compensation. In the continuation of these works, the 3D interconnect coupling in-package effects will be investigated.

The dilemma of assessing the 50%-propagation delay in high-order non-linear interconnects was shown. The role played by the inductive part of transmission line is really important rather than the pure RC-circuit assumption especially for microelectronic interconnects. Numerical modeling of interconnects is a good way to achieve the calculation of SI parameters and reach the existing polynomial theories in complex transfer function. Furthermore, the accurate assessing of 50%-propagation time, rise-time and attenuation by a signal integrity model is necessary to design the new innovative equalization technique introduced [32-35], [71].

Acknowledgements

These research works have been implemented within the frame of the "Time Domain Electromagnetic Characterization and Simulation for EMC" (TECS) project which is part-funded by the Haute-Normandie Region and the ERDF via the Franco-British INTERREG IVA program. Singular acknowledgments are made to LeCroy SARL for the measurements with the SPARQ that were performed and for supplied the expertness in time-domain de-embedding techniques.

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