Compact and Low Loss Microwave Idlers for Low Frequency Integrated Circuits

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Abstract

Two design methodologies for realization of low frequency (less than 20 GHz) compact and low loss microwave idlers have been proposed in this paper. Such idlers can be used for realizing low frequency higher order (6X or more) harmonic mixers or multipliers on monolithic integrated technology. Low frequency higher order harmonic mixers or multipliers are generally avoided due to higher losses and board space consumed by multiple idlers. The present proposed methods of idler design are based on realization of idlers by combining distributed microstrip transmission line and lumped components. The approach helps in transmitting the desired frequency with lower insertion loss and providing more rejection to the undesired frequencies. The design proposal has been demonstrated by designing an idler for 3 GHz local oscillator (LO) side of a 6X harmonic monolithic microwave integrated circuit (MMIC) mixer. This mixer utilizes 6th harmonic of the 3 GHz LO for generating 18 GHz output radio frequency (RF) signal by frequency mixing. The idler for 3 GHz LO rejects direct current (dc), intermediate frequency (IF) and selective even harmonics of LO; 6 GHz, 12 GHz and 18 GHz. On wafer test results of the developed 6X harmonic MMIC mixer has substantiated the idler design.

1. Introduction

Microwave idlers are integral parts of higher order harmonic multipliers and mixers. These are regularly used to selectively suppress unwanted harmonics in resonant terminations to elevate the desired harmonic component and thus improve conversion efficiency. The number of idlers to be used in a circuit depends on the order of mixing or multiplication. The higher the order of mixing or multiplication, the more are the number of idlers used and larger is the footprint area or board space of the circuits.

Idlers are realized using distributed transmission lines or lumped components. Distributed transmission lines require more board space but have lesser losses, whereas, lumped component idlers are compact, but possess higher insertion losses [1]. This issue of space availability versus losses is a major road block in the design of higher order harmonic frequency translation modules [1-3]; which in turn is the reason that 2X harmonic mixer integrated circuits (ICs) are most popular followed by only few instances of realization of 3X and 4X mixers [4-11]. The 2X mixers referred in [4-7] have to utilize only a single resonator or idler and consume lesser board space. Hence, these have been realized as distributed transmission lines to achieve good rejection and lower losses.

At high frequency of operation, typically at millimeter-wave, multiple idlers are feasible as these can be realized using microstrip distributed transmission lines. The 36 GHz, 60 GHz, W-band and 320 GHz 4X mixers of [9-12] use periodicity of the distributed transmission line of a single idler to reject 2X and 4X of the LO frequency. At higher frequencies, distributed transmission lines have smaller wavelengths, thus consuming lesser chip area and inherently possessing lesser losses.

At frequencies lesser than 20 GHz, realization of passive components (like idlers) is usually carried out using lumped R-L-C elements for achieving compactness. This leads to an increase in insertion loss at desired frequency and degradation of rejection at idler frequencies [13-14]. Optimization techniques for idler design [15-16] do not help due to the inherent losses of lumped components.

In this work, two improvement techniques for realizing low loss and higher rejection idlers based on lumped component approach have been proposed and demonstrated using MMIC foundry design kit for a specific case. The idler was used in higher order sub-harmonic I-Q mixer, the on-wafer test result for which has been presented. In spite of idlers being major contributors for conversion efficiency of frequency conversion units, dedicated efforts towards idler design is a less touched upon topic in literature and there are no benchmarks in the said field. Hence, to carry out comparison, the results of the designed multi-frequency idler have been compared with microstrip line based idler design.

The design demonstrated in this paper is an idler designed for LO section of a 6th harmonic (6X) I-Q mixer which uses 6th harmonic (18 GHz) of 3 GHz LO for frequency mixing. The function of this LO section idler is to let propagate the 3 GHz LO frequency with minimum insertion loss and to reject dc, IF (100 MHz) and selective even harmonics of LO; 6 GHz, 12 GHz and 18 GHz (2X, 4X and 6X). The design has been carried out using the

PH25 MMIC process design kit (PDK) of the France foundry, United Monolithic Semiconductors (UMS) and using the software, Advanced Design System (ADS). Figure 1 shows block diagram of the 6th harmonic (6X) mixer.

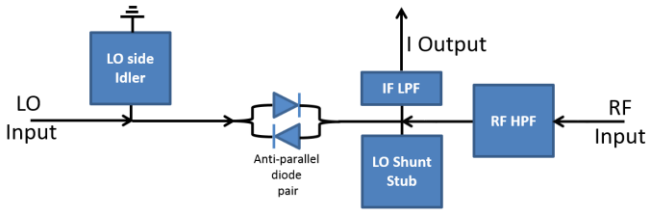

Figure 1: Block diagram of the 6X mixer.

2. Design Methodology

The mixer of figure 1 uses an anti-parallel diode pair for achieving harmonic mixing. For attaining best conversion loss, the IF, RF (6X) and other harmonics of LO i.e. 2X and 4X should be rejected.

Lumped component based idlers are realized by the classical series L-C resonator whose resonating frequency is defined by (1):

$$f_r = 1/(2\pi\sqrt{LC}) \quad (1)$$

Where fr is resonant frequency (Hertz), L is inductance (Henry) and C is capacitance (Farad).

Since lumped components are non-periodic in nature, each frequency to be rejected by the idler would require a different series L-C resonator. Using (1), an idler for suppressing 6 GHz (2*LO) frequency was designed with the UMS foundry kit. Its layout and simulation results are shown in figure 2. The idler which rejects one single frequency, 6 GHz, occupies 0.15 mm x 0.4 mm of area. The rejection achieved at 6 GHz is lesser than 20 dB (18 dB here); the insertion loss and return loss at the desired frequency of 3 GHz is 0.7 dB and 8.9 dB respectively.

2.1. Improvement-1: Idler realization by hybrid approach of microstrip line and L-C Lumped component

A high impedance short length transmission line having electrical length 'θ' lesser than 45 degree can be approximated as an inductor [14, 17] with its inductive reactance 'XL' defined by (2):

$$X_L = w * L_t = Z_{high} * \sin\theta \quad (2)$$

Where 'Lt' is the inductance obtained from the 'θ' length of the transmission line.

$$L_t = (Z_{high} * \sin\theta)/(2 * \pi * f) \quad (3)$$

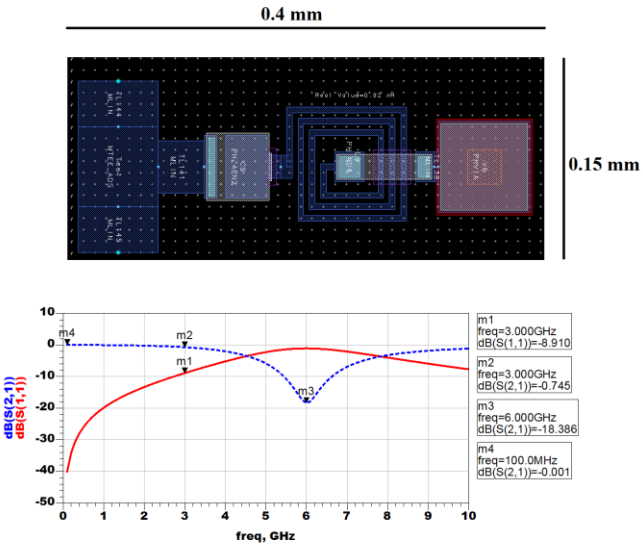

Figure 2: Layout of optimized L-C resonator idler at 6 GHz and its simulated S-parameter response.

Unlike the lumped inductor, value of inductance 'Lt' is dependent on the frequency propagating through the line and electrical length of the line at that frequency. As distributed transmission lines fare lesser resistive losses than lumped components [13], using a short length of transmission line in series with L-C lumped component resonator would retain the low loss properties of transmission lines as well as the compactness of the lumped components. Designers would have a choice of compactness along with better rejection and lesser insertion loss. Figure 3 shows a schematic of such a network. Since, the transmission line is equivalent to lumped inductor 'Lt' in series to L-C (figure 3), effectively it adds to the value of inductance 'Ls' making it 'Ls + Lt'. Hence (1) can be rewritten as:

$$f_r = 1/(2\pi\sqrt{(L_s + L_t) * C_s}) \quad (4)$$

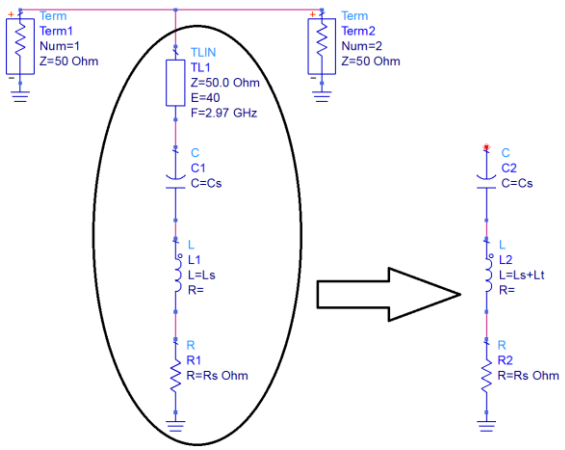

Figure 3: Schematic of hybrid idler approach consisting of both microstrip line and lumped L-C elements.

Therefore, three parameters, namely, 'Ls', 'Lt' and 'Cs' determine the resonant frequency 'fr'. It should be noted that the value of 'Lt' is for 'fr' frequency making it

$$f_r = 1/(2\pi\sqrt{(L_s + (Z_{high} * \sin\theta)/(2 * \pi * f_r)) * C_s}) \quad (5)$$

'θ' is chosen such that after synthesis the actual line length is compact as per the designer's needs. This gives the value of inductance contribution 'Lt' of the transmission line from (3). Next, an arbitrary value of 'C' is selected, from which, the lumped component 'Ls' can be found by extending (1):

$$L_s = (1000/(C * (2\pi f_r)\text{^}2) - L_t \quad (6)$$

Such a network has been synthesized and optimized assuming a 25 degree electrical length of the microstrip transmission line at 6 GHz. Figure 4 shows the schematic of the network and L-C values obtained from (3) and (6). Figure 5 shows the simulated S-parameter response of the network. It may be seen that there is remarkable improvement in the rejection at 6 GHz, from 18 dB (figure 2) to 27 dB (figure 5). But, the insertion loss at 3 GHz is still worse.

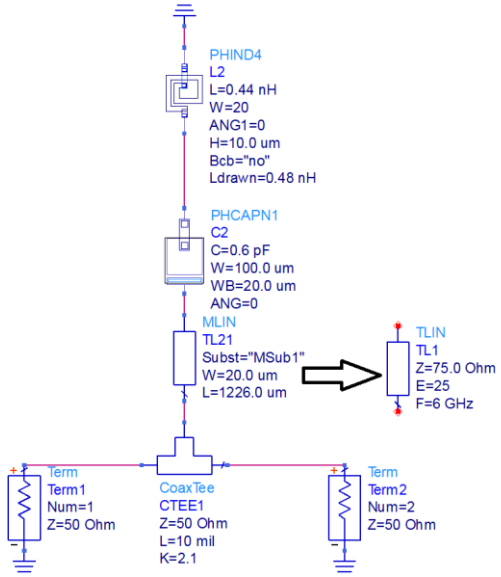

Figure 4: Schematic of optimized 6 GHz hybrid idler.

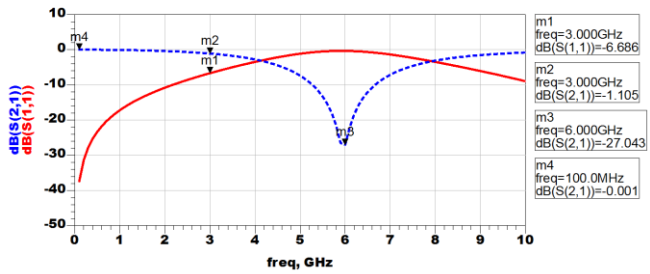

Figure 5: Simulated S-parameter response of the optimized 6 GHz hybrid idler.

2.2. Improvement-2: Improvement using parallel inductor

Although the series transmission line L-C hybrid network discussed above improves the rejection at 6 GHz (2X), it suffers from the following two shortcomings:

(1) The network offers no rejection to dc or IF frequencies. So a separate idler would be required for rejecting dc or IF.

(2) The network suffers from high insertion loss (1.1 dB) at the desired LO frequency (3 GHz in this case).

Adding an inductor in parallel with the L-C network as shown in figure 6 eliminates the two shortcomings. Analyzing the impedance presented by the network of figure 6 in terms of the inductive reactance 'XL' and capacitive reactance 'XC'; the net impedance offered by the network is:

$$Z = [(X_{Cs} + X_{Ls}) * X_{Lp}]/(X_{Cs} + X_{Ls} + X_{Lp} \quad (7)$$

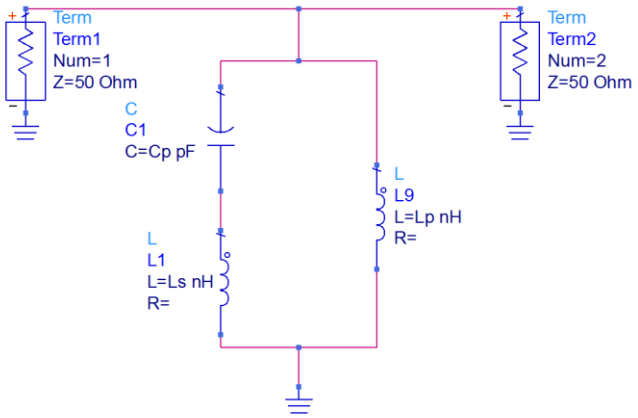

Figure 6: Improved series L-C idler with parallel inductor.

From (7), it can be observed that the impedance offers a short circuit to the following resonant frequencies fr1 and fr2 rejecting these:

$$f_{r1} = 1/(2\pi\sqrt{L_s * C_s}) \quad (8)$$

$$f_{r2} = 0 \quad (9)$$

Where 'fr1' is the L-C series resonant frequency of (1). fr2=0 rejects dc signal and offers significant rejection to all IF frequencies near dc. The third resonant frequency is the most interesting outcome of this network.

$$f_{r3} = 1/(2\pi\sqrt{(L_s + L_p) * C_s}) \quad (10)$$

At frequency 'fr3', according to (7), the network shows open impedance (infinite impedance). (10) can be used to

select the value of 'Lp' such that the network shows an open impedance to the desired LO frequency.

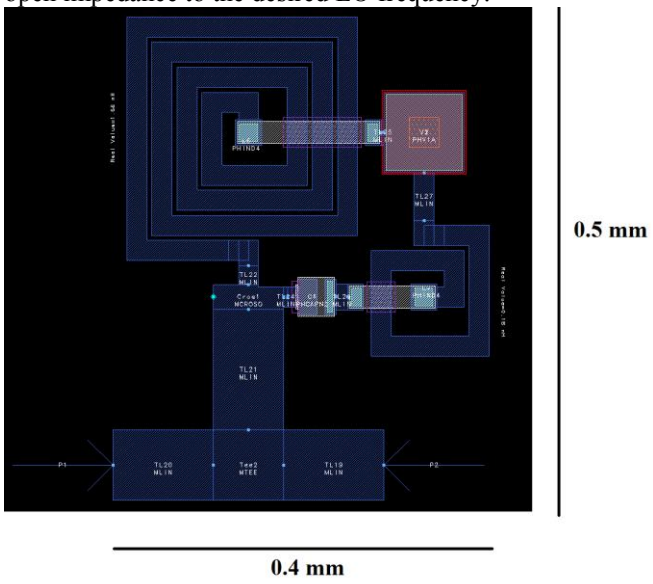

Figure 7: Layout of improved and optimized series L-C idler with parallel inductor.

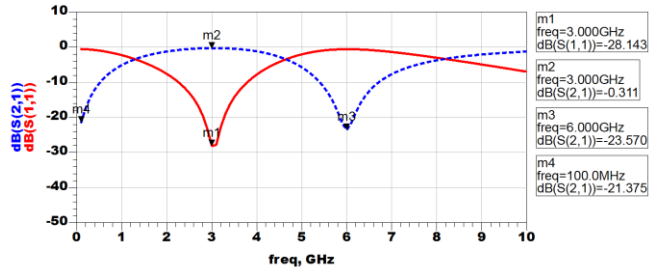

Figure 8: S-parameter simulated response of improved series L-C idler with parallel inductor.

Table 1. Comparison of the original series L-C resonators with the two proposed improvements

Parameter	Series L-C resonator	Series transmission line L-C hybrid idler	Series L-C resonator with parallel L
Insertion loss at 3 GHz	0.75 dB	1.1 dB	0.3 dB
Return loss at 3 GHz	8.9 dB	7 dB	28 dB
Rejection at 100 MHz (IF)	0 dB	0 dB	21 dB
Rejection at 6 GHz (2X)	18 dB	27 dB	23 dB

Using these synthesis formulae, the layout in figure 7 was built for including the shunt Inductor 'Lp' to get minimum insertion loss at 3 GHz LO frequency. Figure 8 shows its simulated S-parameter response. It may be observed that the idler network has become more frequency selective, with significant improvement in return loss (28 dB) and insertion loss (0.32 dB) at LO frequency and good rejection at 2*LO frequency (23 dB). In addition, the network offers considerable rejection (21 dB) to 100 MHz IF frequency. These findings have been tabulated in table 1 for comparison of the two improvements with the series L-C resonator.

3. Development of the improved idler and associated mixer

To realize multi-frequency idler at 2*LO, 4*LO and 6*LO, three L-C series resonant networks would be required along with the parallel inductor for rejecting dc and IF and ensuring acceptable insertion loss at LO. Using the hybrid microstrip line and lumped component approach described in this paper, a network was synthesized for rejecting dc, 100 MHz IF, 6 GHz 2*LO, 12 GHz 4*LO and 18 GHz 6*LO signals and passing 3 GHz LO signal with minimum attenuation. The layout of the network is shown in figure 9 and its s-parameter simulation results are shown in figure 10. As seen, this network consists of four resonators with additional optimized length of transmission lines to decrease the losses. The 4 resonators act as individual idlers to suppress dc/IF, 6 GHz, 12 GHz and 18 GHz signal. The dc idler has been designed in conjunction with (10) to offer minimum attenuation to 3 GHz. The size of the layout is approximately 0.5 mm x 0.75 mm.

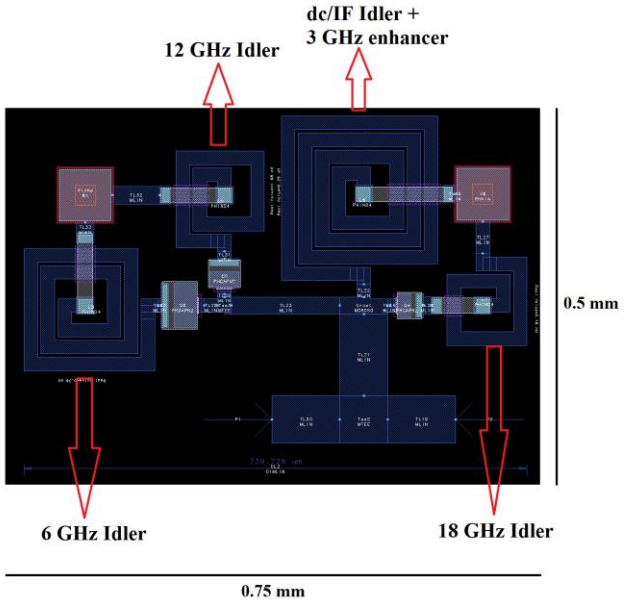

Figure 9. Optimized layout of the multi-frequency idler.

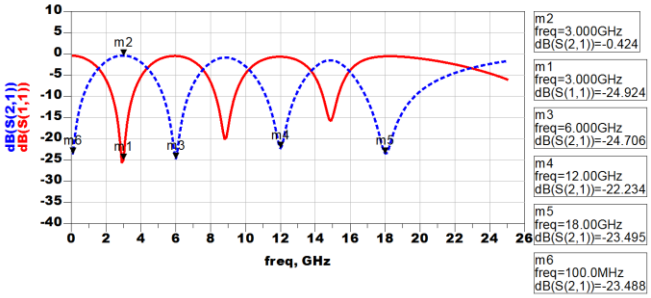

Figure 10: S-parameter simulation of the multi-frequency idler.

As no benchmark exists for the comparison of idlers, a microstrip line shunt stub idler with quarter-wavelength at LO frequency (Figure 11) was designed and optimized. The size of the idler is 1.2 mm x 1.7 mm. Table 2 shows a comparison between the two realization approaches. The proposed idler occupies almost one-fifth lesser board area when compared to the microstrip line idler layout. The improved lumped component idler was used to realize the 6X I-Q Mixer. On-wafer measured up-conversion loss (Figure 12) of the 6X mixer was 15.5 dB with 29 dB of side band rejection and 62 dB LO to RF isolation. Size of the chip is 3.2 mm x 2.6 mm. This conversion efficiency and compact size was possible only due to the compact idler design.

Table 2. Comparison of the proposed improved lumped component based idler with microstrip line based idler

Parameter	Microstrip line Idler	Improved lumped component idler
Insertion loss at 3 GHz	0.1 dB	0.4 dB
Return loss at 3 GHz	42 dB	24 dB
Rejection at 100 MHz (IF)	23 dB	19 dB
Rejection at 6 GHz (2X)	27 dB	24 dB
Rejection at 12 GHz (4X)	23 dB	22 dB
Rejection at 18 GHz (6X)	21 dB	23 dB
Size	1.2 mm x 1.7 mm	0.5 mm x 0.75 mm (5 times lesser)

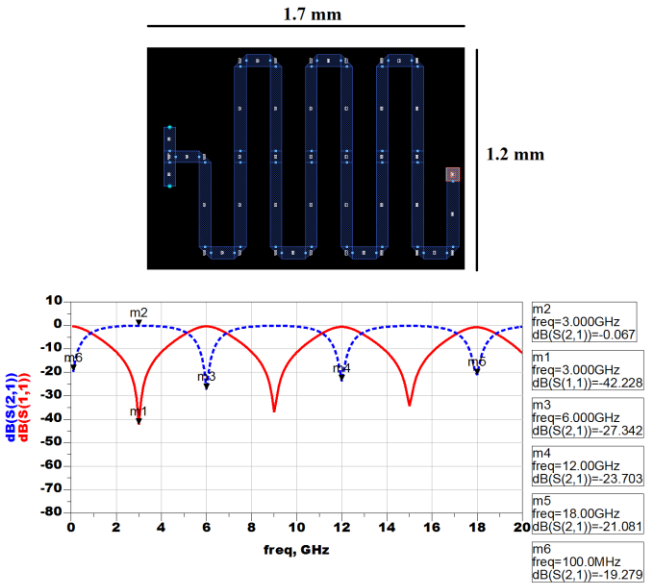

Figure 11. Layout of optimized microstrip line quarter-wave length short stub at 3 GHz and its simulated S-parameter response.

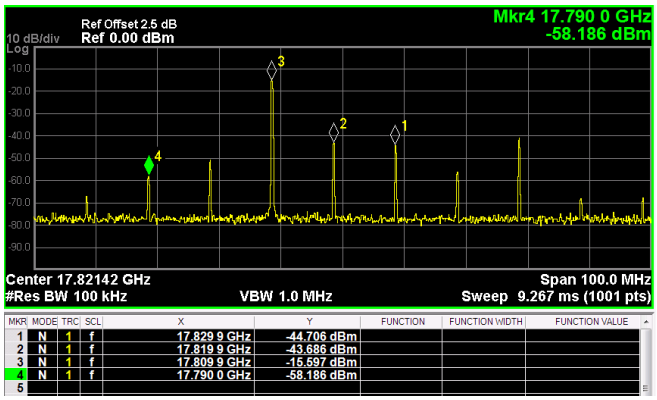

Figure 12. On-wafer measured results of the 18 GHz 6X I-Q Mixer; LO input is 2.97 GHz at +19 dBm, I/Q input is 10 MHz at 0 dBm.

4. Conclusions

In this work, two techniques for realizing low loss and better rejection lumped component idlers have been proposed and demonstrated for 3 GHz LO frequency idler. Using both the techniques together, a multi-frequency idler was designed. The designed idler shows comparable results with microstrip line based idler that tends to be larger in area at lower frequencies. Due to its compact size, the designed idler can be comfortably utilized for realizing complex RF ICs like I-Q mixers in lesser chip area for much higher harmonic mixing and multiplication; ensuring good conversion efficiency at optimal LO power owing to its lower insertion loss.

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